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Publication date:
2016

Document Version
Publisher's PDF, also known as Version of record

Technical University of Denmark

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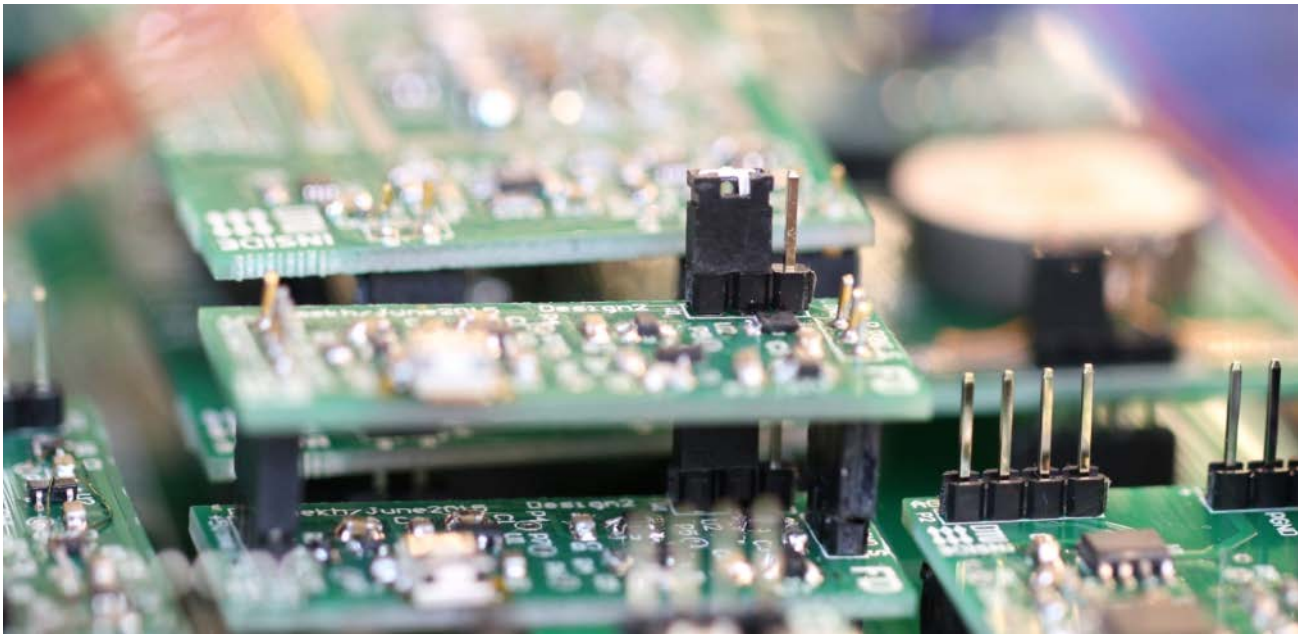

DTU Electrical Engineering
Department of Electrical Engineering

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Inductorless bi-directional piezoelectric transformer-based converters: Design and control considerations

Ph.D. Dissertation, October 2015

Inductorless bi-directional piezoelectric transformer-based converters: Design and control considerations

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Release date:	Date published
Category:	1 (public)
Edition:	First
Comments:	This thesis is submitted in partial fulfillment of the requirements for obtaining the PhD degree at the Technical University of Denmark.

Dedication

Preface

This Ph.D. project "Inductor-less bi-directional transformer-based converters: Design and control considerations" has been carried out at the Electronics Group, Department of Electrical Engineering, Technical University of Denmark (DTU) during the period November 2012 to October 2015. The project was funded by the Danish National Advanced Technology Foundation (HTF), and has been part of the HTF project "PAD Motor- Piezoelectric Actuator Drive to Operate in High Magnetic Fields". The research work was conducted in close collaboration between DTU Electrical Engineering (Elektro) and Industrial partners Noliac A/S, Siemens Health Care and IPU. During the Ph.D. work a research visit with duration of 3½ months was carried out in the Laboratory for Power Management and Integrated Switch Mode Power Supplies, led by Prof. Aleksandar Prodić at Department of Electrical and Computer Engineering (ECE), University of Toronto, Canada.

Acknowledgement

During my Ph.D. I am grateful to all of those who has supported and helped me. It is a matter of great pleasure and privilege for me to be able to express my deep sense of gratitude to my Ph.D. supervisors Prof. Michael A. E. Andersen and Assoc. Prof. Zhe Zhang.

Firstly, I would like to express my deepest gratitude to my supervisor Prof. Michael A. E. Andersen for giving me the great opportunity of Ph.D study and providing me with excellent support for doing this research, for his patience and incessant encouragement. I would also thank Assoc. Prof. Zhe Zhang for his patience, the constructive suggestions and technical discussions during my study. I truly appreciate all of their time, assistance and fully support in all stages of my research. Their advices were immensely helpful for me in carrying out my research.

I would like to thank all colleagues involved in work package 3 (WP3) of HTF2 project, especially Anders R. Steenstrup and Martin Rødgaard from Noliac A/S for their collaboration in designing piezo transformers and constructive discussions during my Ph.D.

I am very thankful to many people at DTU Electronics group both former and current colleagues who all contributed to a pleasant and great working environment.

I thank my fellow T. Gabriel Zsurzsan for his great contribution to my research, all the laboratory works and discussions we have had together in the last three years.

I would like to express my sincere gratitude to Prof. Prodić and all colleagues in the the power lab. in University of Toronto for their valuable discussions during my stay in the power electronics lab., University of Toronto.

I take this opportunity to express gratitude to all my colleagues in the Electronics group for their help and support. Special thanks to Henriette Dalby Wolff, Bertil Morelli and Hans-Christian Nguyen-Andersen for their limitless kindness, patience, and support.

Last but not the least, I would like to thank my parents, and my sisters and brother for supporting me spiritually throughout my Ph.D. and during all my life. I also thank my friends for the unceasing support during my stay in Denmark and during this endeavor. I acknowledge with deep thanks to my love Christian for his great love and support.

Finally, I express my gratitude to all those who helped me directly or indirectly in the successful completion of my Ph.D.

October 2015

Marzieh Ekhtiari

Abstract

Piezoelectric transformers were introduced to the world in 1954 and turned into the best alternative for replacing the magnetic transformers. Recently, the development of research on piezoelectric-based switch-mode power supplies has gathered pace and led to extensive research development. However, this brings an open area for conducting further research which has been subject of this project. The research on this type of power converters are progressive but still very new in the technology to become a successful commercial product. The unique characteristics of piezoelectric transformers i.e. low electromagnetic interference, compact, light, high power density and low cost allows for promising market in the near future. The piezoelectric transformer technology has the potential to be used in various applications e.g. motor driver for magnetic resonance imaging scans, the electronic ballast for fluorescent lamps, backlight for LCD displays in notebook computers.

Piezoelectric ceramic devices vibrate at their mechanical resonance. The operating principle of the piezoelectric transformers is based on electromechanical energy conversion. There is electromechanical coupling between the primary- and secondary-side of piezeo ceramic, where the primary acts as a piezoelectric actuator and the secondary acts as a piezoelectric transducer. Therefore, piezoelectric transformers can be used as a replacement of resonant circuits in the power converters. This introduces piezoelectric transformers as applicable candidates for applications that have a high sensitivity to electromagnetic interference. The nonmagnetic bidirectional piezoelectric transformer-based switch-mode power supplies as the topic of this thesis is one of these applications.

The dissertation presents the design, control and implementation of inductorless switch-mode power supplies employing piezoelectric transformers. The main focus of this research is on the functionality of the piezoelectric transformer-based power converters and applying control techniques in order to exploit advantages of the piezoelectric transformers for the power converters. Therefore, the research is devoted to stepwise development of all parts of the iductorless piezoelectric transformer-based switch-mode power supply. The developments have been mainly on the transformer design for internal resonant current sensing, increasing their capability in transferring energy and soft switching, following changes of the piezoelectric transformer in order to control operation of the piezoelectric transformer for the benefit of the power converters, digitizing control system, applying new control techniques compared to previously applied methods, implementing dynamic optimum dead time detector applicable for switch-mode power supplies, optimum phase

detector, bi-directional wide bandwidth current sensor and a comprehensive analysis of piezoelectric transformer-based switch-mode power supplies for zero-voltage switching, where all finalized with improving the unidirectional topology with resistive and passive rectifiers as well as bi-directional topology with a capacitive load.

The investigation of the piezoelectric transformers in terms of sensing the resonant current and increasing their capability of handling high power was carried out in collaboration with the project's industry partner. New samples of piezoelectric transformers were designed, fabricated and tested. Experiments showed promising results on sensing the resonant current, but could not be used for the control system in this research since having both sensing electrode and zero-voltage switching could not be obtained in one package. Moreover, a progress of increasing power capability of piezoelectric transformer's was a step forward to overcome the limitations in the technology of the piezoelectric transformers.

Operation of unidirectional topology deals with finding solutions for advance control of piezoelectric transformers in terms of operating under various load, frequency and temperature changes. In order to follow changes in the characteristic of the transformers and control their operation, a digitized self-oscillating loop designed and implemented. The main advantage of the digitized self-oscillating loop is that the time delay inside the loop is able to be changed with the resolution of 1 ns. This provides the possibility of sweeping the operating point on the characteristic over the frequency range by very fine frequency steps where considerable changes in the output voltage of the transformer are visible. This is done by shifting the gate voltages of the switches versus the resonant current.

Having access to the mechanical resonance of the piezoelectric material inside the piezoelectric transformer, known as "resonant current" in its equivalent electrical circuit, simplifies the control system of the entire converter. Therefore, attempts were made to find solutions for sensing the resonant current over the whole or part of the switching time period. The first approach was to design a piezoelectric transformer with feedback to sense the mechanical resonance. The second approach was to design a current sensor for measuring the input current to the transformer which is equal to the resonant current during the on time of the switches. The second approach requires a wide bandwidth bi-directional current sensor to be able to operate in the presence of the high common-mode voltage. Part of this research allocates to implementation of the current sensor.

A new method for optimizing the dead time in every switching cycle is proposed. The dynamic optimum dead time detector starts to detect the time point where the switching voltage reaches the rails or passes through its local maxima. This results in the minimum or the optimum dead time between the switching transitions and further expanding the duty cycle of the switches in order to provide more energy to the converter. The advantage will be reduction of the start-up time in the converter and the switching losses.

The main achievement of this research is a new implementation of bi-directional piezoelectric transformer-based switch-mode power supply with two configurations. This implementation is applicable for the control system of switch-mode power supplies, specially resonant power converters. Finally, the outcome of the research

is implemented and tested in the final prototype with combining all the designed sub-circuits to investigate the bi-directional functionality of the power supply, which resulted in a successful outcome in the control techniques.

Keywords: Piezo transformer; PT-based SMPS; zero-voltage switching; optimum dead time; phase shift control; self-oscillating loop; bi-directional converter; inductorless resonant converter.

Resumé

Piezoelektriske transformatorer blev introduceret i 1954 og har siden vist sig at være et godt alternativ til magnetiske transformatorer. For nylig har udviklingen af forskningen i switch-mode strømforsyninger baseret på piezoelektriske transformatorer taget fart og ført til en omfattende udvikling. Dette har medført et åbent område for at udføre yderligere forskning, hvilket har været genstanden for dette projekt. Forskningen i denne type effektomformere er stadig på et tidligt stadie i forhold til at blive et vellykket kommercielt produkt. De unikke egenskaber for en piezotransformator: lav elektromagnetisk interferens, lav volumen og vægt, høj effekttæthed og lav pris giver mulighed for et lovende marked i den nærmeste fremtid. Piezoelektriske transformatorer har potentialet til at blive anvendt i mange forskellige applikationer f.eks. motor-drivere til magnetisk resonans scannere, elektronisk ballast til lysstofrør og baggrundslys til LCD-skærme i bærbare computere.

Piezokeramiske enheder vibrerer ved deres mekaniske resonans. Piezotransformeres funktionalitet er baseret på elektromekanisk energiomsætning. Der er elektromekanisk kobling mellem primær- og sekundær-siden af en piezokeramisk enhed, hvor primærsiden fungerer som en piezolektrisk aktuator, og sekundærsiden fungerer som en piezoelektrisk transducer. Derfor kan piezotransformatorer anvendes som en erstatning for resonanskredsløb i effektomformere. Dette introducerer piezotransformatorer som mulige kandidater til applikationer, der har en høj følsomhed over for elektromagnetisk interferens. Emnet for denne afhandling er netop en sådan applikation, nemlig den ikke-magnetiske tovejs piezotransformer-baserede switch-mode strømforsyning.

Afhandlingen præsenterer design, regulering og implementering af piezotransformerbaserede switch-mode strømforsyninger, der ikke gør brug af spoler. Det primære fokus i denne forskning er på funktionaliteten af piezoelektrisk-baserede effektomformere og anvendelsen af reguleringsteknik til at udnytte fordelene ved de piezoelektriske transformere i strømforsyninger. Derfor er forskningen helliget den gradvise udvikling af alle dele af spoleløse piezotransformer-baserede switch-mode strømforsyninger. Udviklingen har primært været på transformerens design med henblik på intern resonansstrømmåling, forøgelse af den maksimale effektomsætning samt soft-switching. Derudover er følgende blevet udført: ændringer af piezotransformeren for at kunne kontrollere transformeren bedre med henblik på dennes brug i effektkonvertering, digitalisering af regulatoren, anvendelsen af nye reguleringsteknikker sammenlignet med tidligere anvendte regulatorer, implementering af dynamisk optimal dødtidsdetektor til brug i switch-mode-strømforsyninger, optimal

fase detektion, bidirektional bredbåndet strømsensor og en omfattende analyse of piezotransformer-baserede switch-mode strømforsyninger for zero-voltage switching. Slutteligt er den unidirektionale topologi blevet forbedret med resistive og passive ensrettere samt den bidirektionale topologi med kapacitiv last.

Undersøgelsen af piezo-transformere med henblik på måling af resonansstrømmen og forøgelsen af den maksimale effekthåndtering blev udført i samarbejde med en ekstern samarbejdspartner fra industrien. Nye prøveemner af piezotransformeren blev designet, fabrikeret og testet. Eksperimenterne viste lovende resultater for måling af resonansstrømmen, men dette kunne ikke blive brugt i reguleringssystemet i dette forskningsprojekt, da det ikke var muligt at have både en målelektrode og mulighed for zero-voltage switching i samme pakke. Opnåelsen af en højere maksimal effekthåndtering er et skridt i den rigtige retning for at overkomme nogle af de teknologiske begrænsninger for piezotransformere.

Den unidirektionale topologi blev undersøgt med henblik på at finde nye avancerede metoder for regulering af piezoelektriske transformatorer med henhold til drift under forskellige belastninger, frekvens- og temperatur-ændringer. En digital selvoscillerende reguleringssløjfe blev designet og implementeret for at kunne følge ændringerne i transformerens karakteristika over de varierende driftsforhold. Denne reguleringsmetode har den store fordel at tidsforsinkelsen inde i reguleringssløjfen kan ændres med en opløsning på 1 ns. Dette giver mulighed for variere arbejdspunktet, og dermed transformatorens karakteristika, med høj præcision ved at ændre på driftsfrekvensen. Betydelige ændringer i udgangsspændingen blev observeret ved at ændre arbejdspunktet. Dette blev gjort ved at ændre på gate-spændingen på kontakterne i forhold til resonansstrømmen.

Ved at have adgang til viden om den mekaniske resonans af det piezoelektriske materiale, også kaldet resonansstrømmen i det ækvivalente elektriske system, kan reguleringssystemet for hele strømforsyningen forsimples betragteligt. Derfor er det blevet forsøgt at finde en løsning på at måle resonansstrømmen over hele skifteperioden, eller dele deraf. Dette blev gjort på to måder: ved at designe en piezotransformer med feedback fra den mekaniske resonans og ved at designe en strømsensor for at måle indgangsstrømmen til transformeren, som svarer til resonansstrømmen når kontakterne er tændte. Den sidstnævnte løsning kræver en bidirektional strømmåler med høj båndbredde for at kunne bruges ved tilstedeværelsen af den store common-mode spænding. En del af dette forskningsprojekt beskæftiger sig med implementeringen af strømsensoren.

En ny metode til optimering af dødtiden i hver skifteperiode er blevet foreslået. Den dynamiske optimal-dødtidsdetektor registrerer tidspunktet hvor skiftespændingen når forsyningsspændingen eller passerer dens lokale maksimum. Dette resulterer i den minimale (eller optimale) dødtid mellem skifteovergangene og øger dermed udnyttelsesforholdet af kontakterne og mere energi kan dermed leveres til konverteren. Fordelene ved dette er en reduktion af opstartstiden for konverteren og skiftetabene.

Det hovedsagelige resultat af dette forskningsprojekt er en ny konfiguration af en bidirektional piezotransformer-baseret switch-mode strømforsyning med to konfigurationer. Denne implementering kan bruges til reguleringssystemer til switch-mode strømforsyninger - især resonanseffektkonvertere. Endelige er resultaterne af denne forskning implementeret og testet i den endelige prototype, der kombinerer alle

de designede undersystemer for at undersøge funktionaliteten af den bidirektionale strømforsyning, hvilket mundede ud i et succesfuldt reguleringssystem.

Contents

Acronyms

CCFL cold cathode fluorescent lamp

CEZC current estimation zero crossing

CT computed tomography

DAC digital-to-analog converter

DB digital block

DDL digitized delay line

DEAP dielectric electro active polymers

DT dead time

EMI electromagnetic interference

FPGA field-programmable gate array

HS high-side gate voltage

IC integrated circuit

IDE interleaved interdigitated electrode

LPF low pass filter

LS low-side gate voltage

MOSFET metal-oxide-semiconductor field-effect transistor

MRI Magnetic resonance imaging

ODL optimum delay line

ODT optimum dead time

PAD Piezo Actuator Drive

PMA piezoelectric multilayer actuators

PT piezoelectric transformer

RF radio frequency

SMPS Switch-mode power supply

ZVS zero-voltage switching

List of Figures

Chapter 1

Introduction

1.1 Background and Motivation

This Ph.D. project is part of the Piezo Actuator Drive (PAD) motor project. The target of this project is the development of the first fully non-ferromagnetic motor with a torque of several newton meter (N.m). PAD [1] is introduced for high value-added medical applications, primarily within the medical imaging market for treatment tables in MRI and computed tomography (CT), and secondarily for medical infusion pumps. The core of the PAD technology consists in a principle of transforming the linear motion, periodic elongation, of high performance piezoelectric multilayer actuators (PMA) into powerful, precise, dynamic and controllable continuous rotation. The creation of the motor based on the PAD principle, requires the development of innovative driver solutions for the piezoelectric actuators. There are some limitations in the current treatment tables e.g. motors cannot operate in the presence of strong magnetic field inside the MRI room. Furthermore, imaging and motor operation cannot take place simultaneously. This project has aimed for overcoming the existing limitations by designing the PAD motor and a driver for running the motor to be able to operate inside the strong electromagnetic fields. Figures 1.1 and 1.2 show an expanded view of a PAD motor with illustrating the location of piezoelectric actuators.

The key for the development of a driver capable of functioning inside the strong electromagnetic field, e.g. 7 Tesla, without interfering the image processing of the MRI is to exhibit nonmagnetic behavior. For this purpose, no magnetic components, i.e. inductors, magnetic transformers can be used in the driver. Furthermore, implementation of energy recovery strategies will be the key to obtain a highly efficient driver system. This imposes strict requirements on its design and calls for advanced control schemes. Requirements for energy recovery and driver efficiency demand innovative solutions beyond existing state-of-the-art technology for the design of the PAD motor.

PTs are suitable candidates for addressing this challenge. This leads into replacement of magnetic transformers with PTs. Furthermore, utilizing PTs reduces size,

Figure 1.1: PAD motor.

weight and cost of the driver compared to the use of bulky inductors and magnetic transformers. Presently, nonmagnetic PT-based SMPS are new in the technology. Additionally, the bi-directional topology for energy recovery from the load is not commonly used in the PT-based converters since it first requires overcoming challenges in the unidirectional configuration.

1.2 Thesis scope and objectives

The goal is to reduce the size, increase the efficiency and energy recovery from the piezo actuator. The scope of this thesis is to present the research carried out for the duration of the project, from November 2012 to October 2015. Most of the scientific results of the research have been published or submitted in the form of peer reviewed conference and journal papers, as well as filed patents. The publications form a significant part of this thesis and are included in the Appendices. The thesis supplements already published and thereby presents a more coherent and complete overview of the research work and the results obtained during the course of the Ph.D. project. In this research, focus will be on the nonmagnetic driver for the piezo actuators and on employing energy recovery from the capacitive actuators. Therefore, piezoelectric transformer-based power converters are used for driving piezoelectric actuator drive motor in the presence of high electromagnetic field. The perspective of the project is shown in Fig. 1.3. An extensive introduction to this project is introduced in the appendix A.

The preliminary objective of this Ph.D. thesis is to investigate nonmagnetic, energy efficient, and bi-directional PT-based SMPS. This offered the possibility of investigation of several key areas of the PT-based power converters in the same line of the project's goals, which in particular are:

- Development of a driver with nonmagnetic properties.

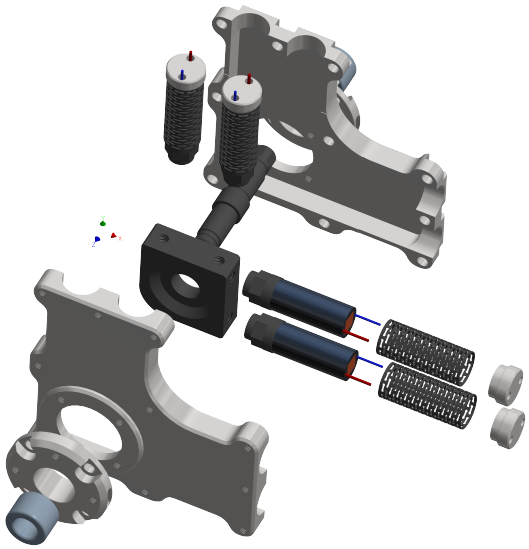


Figure 1.2: Four piezo actuators inside the PAD motor.

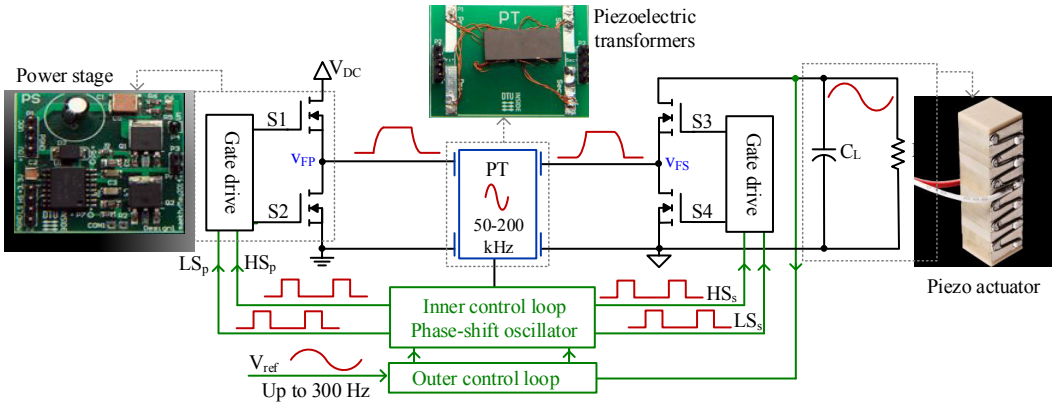


Figure 1.3: Total perspective of the project.

- Development of a self-oscillating loop to control the operating point of the PT.
- A control method comprised of digital and analog techniques.
- Bi-directional power flow.
- Successful demonstration of unaffected driver performance and MRI imaging quality when testing the prototype in a Siemens Magnetom Vision MRI treatment table.

1.3 Thesis structure and content

The structure and content of this Ph.D. thesis are visualized in Fig. 1.4. Furthermore, the published or submitted conference and journal papers are illustrated in this flow chart.

Chapter 1 briefly introduces the background and motivation, scope as well as the objectives of the project. The overview and state-of-the-art are discussed in Chapter 2.

Chapter 3 discusses the research related to the unidirectional PT-based switch-mode power supplies including self-oscillating control loop, combination of digital and analog control for the phase shift loop, and digital control implementation.

Chapter 4 discusses the research related to the bi-directional topology and control techniques.

The results of the test of the designed converter inside the strong magnetic field is provided in Chapter 5.

The thesis is finalized with conclusions and future works. The purpose of this thesis is to provide a condensed and coherent overview of the research and results obtained in the thesis. Relevant publications are included in the Appendices.

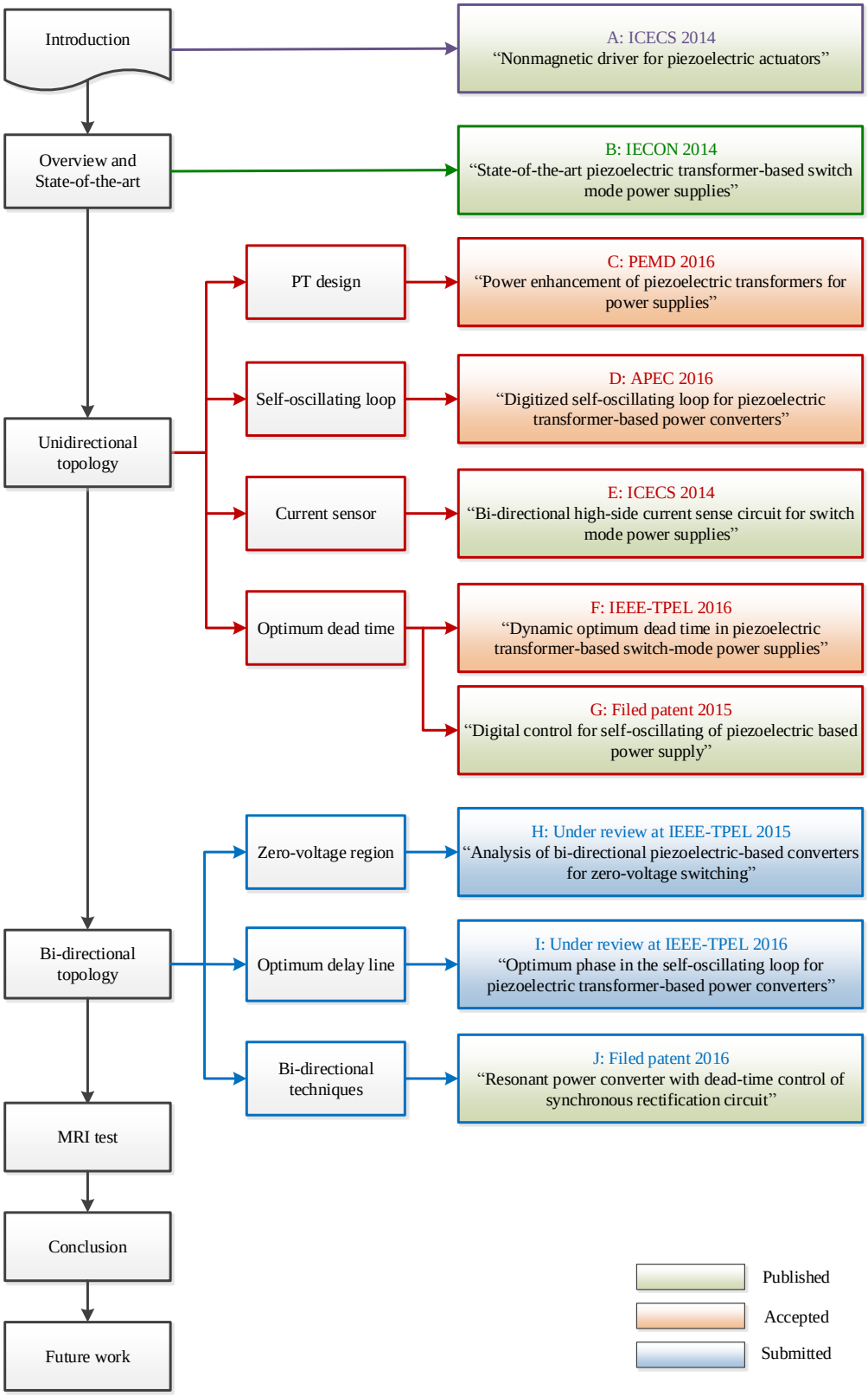


Figure 1.4: The structure of the thesis.

Chapter 2

State-of-the-art

An introduction to the state-of-the-art on PT-based SPMS is described in this Chapter as well as in the Appendix B.

2.1 Ceramic piezoelectric transformers (PTs)

Presently, development within PTs has been increasing with regards to smaller size, lighter weight, lower cost, lower electromagnetic interference (EMI), higher power density, and higher efficiency compared to the conventional transformers [2–4]. PTs are initially considered as high-voltage transformer devices [5]. Employment of PTs has become popular since they allow the replacement of magnetic transformers with a ceramic components [3]. PT is typically, lighter, cheaper, smaller and more efficient compared to a magnetic transformer, but a magnetic transformer has the ability to function over a wide range of load conditions. The PT has the advantages of inherently sinusoidal operation, nonflammability, and no electromagnetic noise. The choice of transformer depends on various parameters including size, efficiency, load range, output power level, application, etc. For example, usage of PT for driving cold cathode fluorescent lamp (CCFL) as a backlight source in notebook computers eliminates the need of having a ballasting element between the PT and the CCFL, when the lamp strikes [6, 7]. This is due to PT's unique gain characteristic with load. PT's provides high quality factor (Q) and high gain under no-load condition [8, 9].

Developing an electrical circuit model for the PT is useful to predict PT's performance in a system [8, 10]. The model shown in Fig. 2.1 is often used to describe the behavior of a PT close to the resonant frequency. The mechanical piezoelectric gain near a single resonant frequency can be modeled by a series R, L, C circuit in the electrical equivalent model.

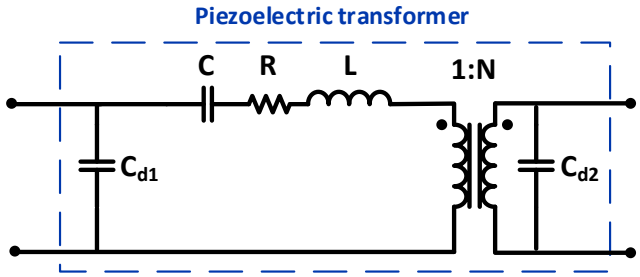


Figure 2.1: Equivalent piezoelectric transformer circuit model.

2.2 PT-based SMPS

The development of PT-based switch-mode power supplies has gathered pace in recent times due to their smaller size, lighter weight, lower cost, lower EMI, higher efficiency in comparison with converters using conventional magnetic transformers [2, 3, 11, 12]. Recently, inductorless PT-based SMPS are being used because of their specific usage in nonmagnetic applications [13–16]. The PT is normally operated in a narrow frequency band around its fundamental or primary resonance frequency with the matched load coupled to the output of the transformer. The optimum operating frequency or excitation frequency shows strong dependency on different parameters such as temperature, load, fixation and age [17]. Thereby, it is a significant challenge to maintain the excitation frequency applied to the input section of the PT at the optimum frequency during operation of the power converter, where aforementioned parameter changes.

2.2.1 Inductorless unidirectional PT-based SMPS

PT-based switch-mode power supplies are typically used in the form of a unidirectional topology to provide power to a resistive load or charging a capacitive load [17–21]. A PT reaches its maximum efficiency when being operated in a frequency slightly above its resonance [22]. Therefore, it is important to keep the switching frequency above the PT's resonance, despite of dynamic changes in its resonant frequency [23]. The best approach has been designed by a self-oscillating loop to follow changes of the PT for having desired functionality of the converter in terms of efficiency [22]. In order to avoid large switching losses in the inductorless PT-based power converters, the employed PT should have native zero-voltage switching (ZVS) property, i.e. ZVS factor larger than 100% [17, 24], and exploit this property to obtain ZVS for the input driver's switches. ZVS operation of the input switches has traditionally been achieved by adding an external inductor in series with the PT to ensure the input of the PT appears inductive across relatively large frequency range and allow the output capacitance of the switches alternatively charge and discharge without a large power loss.

2.2.2 Bi-directional topology

Up to now, bi-directional PT-based converters are not commonly used. A bi-directional PT-based converter has been implemented for dielectric electro active polymers (DEAP) actuators with some shortcomings in the control loop, specially due to the high output voltage application [22]. In the previous research, the control technique for applying phase shift in the loop has been implemented for a bi-directional converter through an analog circuit by detecting the peak value of the resonant current [25]. This method of implementation in general and specifically in bi-directional operation cannot cover the full range of the phase shift in the closed-loop operation [26].

2.3 Zero-voltage switching

ZVS is a form of soft switching considered in this research. In the PT-based SMPS, the ZVS is investigated in two domains: firstly, capability of the PT in providing conditions for ZVS in the converter and secondly, ZVS for the switches.

Having a PT which ensures the ZVS for the switches highly depends on the PT's parameters i.e. PT's coupling coefficients, turn ratio and capacitor ratio [18,24,27]. To evaluate the ZVS capability of the PT, a ZVS factor was defined for PTs which provides the worst case for obtaining ZVS in terms of soft switching capability. This means that if ZVS is obtained for the PT connected to the matched load [4, 10], it will be obtained for other loads as well [24]. The modified explanation of the approximated ZVS factor is expressed based on empiric analysis of ZVS [17].

For the switches in the power converters, achieving ZVS reduces the switching losses [16]. Therefore, different approaches have been performed to obtain the ZVS capability. A commonly used solution is to place an inductor in series with the PT in order to pump a sufficient current into the PT's input capacitor during the dead time. This approach resulted in extra size, expense and EMI noise. However, adding an inductor in series with the PT facilitates achievement of the ZVS. In case of having optional frequency and dead time, obtaining the ZVS depends on several factors, e.g. the load condition [13], and the PT's ZVS factor [17]. For the inductorless PT-based SPMS, the solution of adding a series inductor cannot be considered [28]. Thereby, it is important to provide a situation that ZVS can be achieved for the power converter [28, 29]. Therefore, it is advantageous to apply advanced control techniques to obtain the ZVS in the PT-based SPMS.

2.4 Control methods

The PT's characteristic changes due to the temperature and age [27]. The PT's voltage gain, resonance frequency and efficiency change with changes in the load, temperature and the output voltage level [2, 4, 30]. For example, power loss inside the transformer causes self-heating and consequently temperature increase. This results in decrease of voltage gain and the resonant frequency. For a fixed switching frequency, this easily shifts the switches out of the ZVS region and consequently,

decreases the output voltage and the efficiency [27, 31–33] In order to find the most efficient operating point of the PT for a specific operating condition i.e. load, output voltage level and temperature, suitable control techniques should be employed.

A closed loop control based on the phase shift self-oscillating loop was used in the previous research [12, 18, 22, 23]. Furthermore, the closed loop control strategies allowing the ZVS operation of the converter was suggested in [34, 35]. The self-oscillating control loops were used for the first time for the inductorless PT-based SMPS [23].

A bi-directional configuration was implemented for the PT-based power converter with a load of DEAP [18, 25]. The phase shift control was employed in order to avoid the use of two different PTs for achieving ZVS in both forward and reverse energy flow. Experiments substantiate the claim of bi-directional power converters with active phase shift controls and utilization of one PT [22, 23, 25].

2.5 Summary

This chapter had a brief introduction to the PT-based SMPS. The state-of-the-art solutions were described for the PT-based converters in this Chapter as well as in the Appendix B. The challenges impose strict requirements on the design of this type of converters. The outcome of the literature review for the state-of-the-art is published as a conference paper, enclosed in the Appendix B, which gives an overview of the existing knowledge.

Chapter 3

Unidirectional topology

We realize that efficient and compact nonmagnetic drivers will have a revolutionary impact on eliminating the technological limitations for medical applications. Nonmagnetic piezoelectric actuator drive is the only form-fit drive solution currently available for the development of high performance nonmagnetic motors. This chapter deals with contribution of this research on stabilization and efficiency increase of PT-based SMPS. In addition to what is presented in this chapter, more detailed information may be found in Appendices C, D, E, F, and G.

3.1 PT design

PTs use electromechanical coupling between the primary and secondary sides compared to conventional transformers with electromagnetic coupling. Mechanical resonance inside the PT occurs at multiple standing-wave frequencies (f_n) based on the transformers dimensions and material. Voltage gain is normally a function of the PT material coefficients, the number of primary and secondary layers, the thickness of layers and the overall length. The PT's input and output capacitances, C_{in} and C_{out} respectively, are formed as a result of the multi-layer construction of the primary dielectric layers and the electrodes.

Contribution of this research was not directly focused on designing the transformers. However, some effort was allocated collaborating with our industrial partner, Noliac A/S, on designing the transformers for achieving the desired performance for this application in terms of ZVS and power transferring properties. The PT design was performed through three prototypes that will be described in the following subsections.

3.1.1 Design considerations

The effort for designing PTs in this research was mainly in three domains i.e. the ZVS capability, power enhancement of the transformer, and an internal sensor for

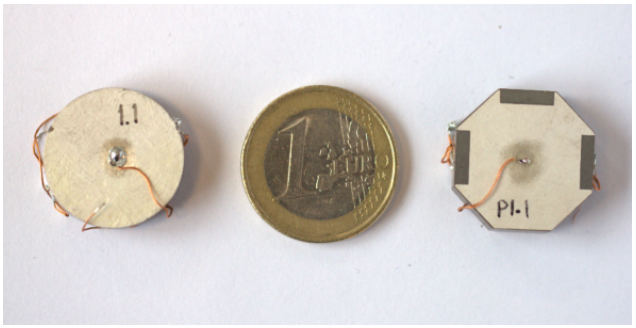


Figure 3.1: Two types of radial mode PTs with different geometry produced during the research.

resonant current for sensing the electromechanical resonance of the PT.

3.1.2 ZVS property

In order to reduce switching losses in an inductorless power converter, PT should be capable of having native and reliable ZVS property i.e. ZVS factor larger than 1 [18,24]. Despite of theoretical analysis of ZVS properties of a PT, there is a trade-off between the ZVS factor and the power density in practice. In this research the effort was to design a PT with a ZVS factor close to or above 1. The key was to have the same ZVS factor for forward and reverse power flow. Therefore, there should be a trade-off between electromechanical and piezoelectric coupling coefficients in the primary- and secondary-side of the transformer [18].

In the first prototype the effort was to increase the power density of the transformer and fulfilling inherent capability of the PT for obtaining ZVS. This is done with attention to have the same coupling coefficient in the primary- and secondary-side of the transformer in order to achieve ZVS for the bi-directionality topology. Increasing the power density of the transformer results in higher power throughput, but it is limited by design method and production factors. Figure 3.1 shows two types of radial mode PTs with different geometries. The PT with octagon geometry was not a successful design because soft switching could not attained for this samples. The radial mode PT with circular geometry was quite successful in obtaining ZVS and functionality. The only issue was that this prototype of PT cannot handle the power above 2 watts.

3.1.3 Power enhancement

A measurement showed that a peak power of approximately 100 watts is required to drive a piezoelectric stack. This means that the PT to be used in the power supply should be capable of transferring the demanded power to the load. The radial piezoelectric transformer of Figure 3.1 could not handle more than 2 watts. Obviously, such as low power capability leads the transformer to operate above its power rating threshold. As a consequence, the temperature inside the transformer increases significantly. This motivates a change of the resonant frequency, decrease

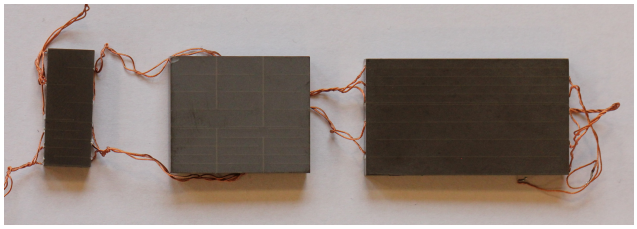


Figure 3.2: The second prototype of PTs, designed in order to increase the output power.

of the transformer efficiency, and increase of the risk of cracking. This brought a further challenge to this research.

In order to increase power transmission capability of the transformer two solutions are found. The first solution is to combine multiple PT-based converters together in order to sum up the output power. This approach requires self-oscillating loop for each individual PT to follow changes of the PT's operating point with regards to temperature and load. Moreover, it requires complicated control system in order to control the connection of transformers and provide the desired output voltage. This solution was beyond the scope of this research, since there were still fundamental issues in control of one single PT inside the driver. Another solution is to mechanically combine different modules of PTs and make a single PT with higher power throughput. This approach is tried by design and fabrication of three sample types of interleaved interdigitated electrode (IDE) PTs [22, 31]. Figure 3.2 shows these PT samples. The peak power that can be handled by the new designed PTs is 5 watt. More details about enhancing power of the PT in this design can be found in the Appendix C.

The designed piezoelectric transformers i.e. radial modes and different type of rectangular PTs are used during the entire research for various experiments.

3.1.4 Internal sensor for resonant current

In the PT-based converters typically there is no access to the inside of the package of the PT to sense the resonant current of the PT. However, there is a need to sense the electromechanical resonance of the PT for controlling its operating point. To address this issue a sensing circuit is used in the current self-oscillating loop called current estimation zero crossing (CEZC) circuit, shown in Fig. 3.3, comprising of an amplifier, a low pass filter (LPF) and a comparator [23]. In order to smooth the resonant current, the estimated current is passed through a LPF to filter out harmonics and switching noises. The issue about this sensor is that there is no information available about the precise zero crossing time point of the resonant current due to delay added by LPF. Knowing the exact zero crossing time point of the resonant current is in the control technique used for the optimum dead time (ODT) and digital blocks in terms of ODT and ZVS (Fig. 3.26 in the Section 3.5).

To solve this problem, a PT with an auxiliary tap or feedback electrode was suggested to be designed. The idea was to have a PT with an electrode output that

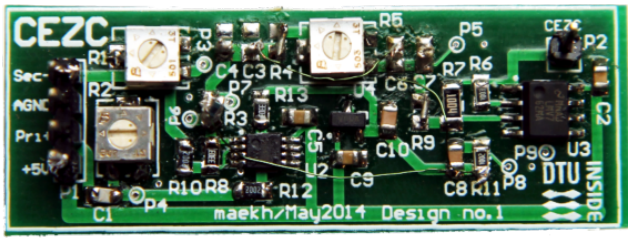
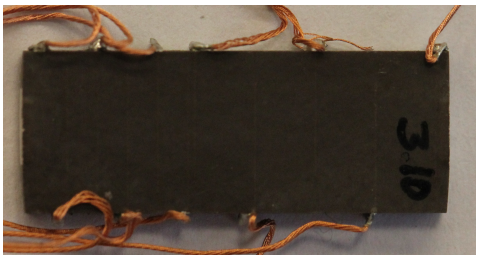
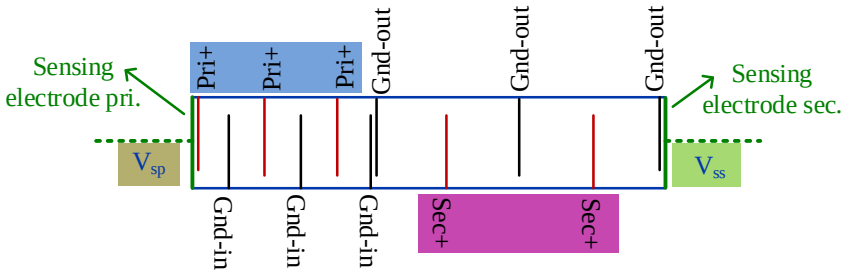


Figure 3.3: The resonant current estimation board.



(a) Prototype



(b) Layout

Figure 3.4: PT with sensing electrode, the first prototype.

feeds back the electromechanical resonance inside the PT through a piezo layer in the primary- or secondary-side of the PT in order to have sensorless resonant control system. However, PTs with feedback tap solutions to monitor the resonant current have been presented in previous research [36,37]. In this research two prototypes of transformers were produced for this purpose. Figure 3.4 shows the first prototype of the PT with isolation between its primary- and secondary-sides. Moreover, its layout with feedback electrode is shown. In this prototype voltage amplitude of the sensed resonance was at the noise level and could not be used for control purposes. The measurement is shown in Fig. 3.5. An advantage of this design was that the PT had inherent ZVS property.

Figure 3.6 shows auxiliary tapped PT in the second prototype. The equivalent electrical circuit model and measurements are shown in Figs. 3.7 and 3.8, respectively. In this prototype the sinusoidal output waveform from the auxiliary tap was quite above the noise level, shown in Fig. 3.8, and could be used for the control

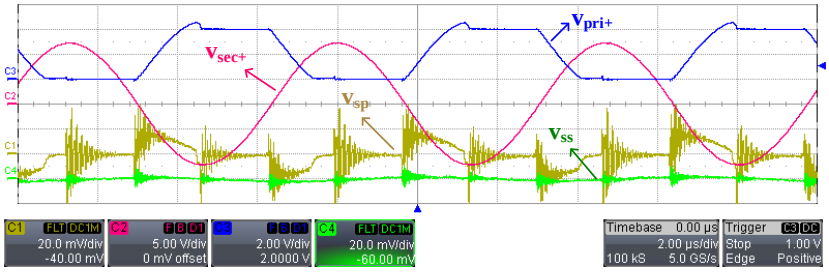
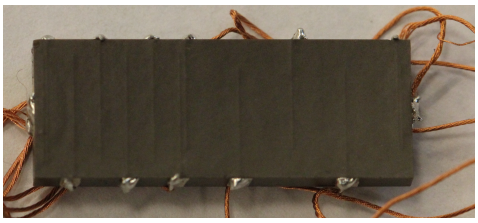
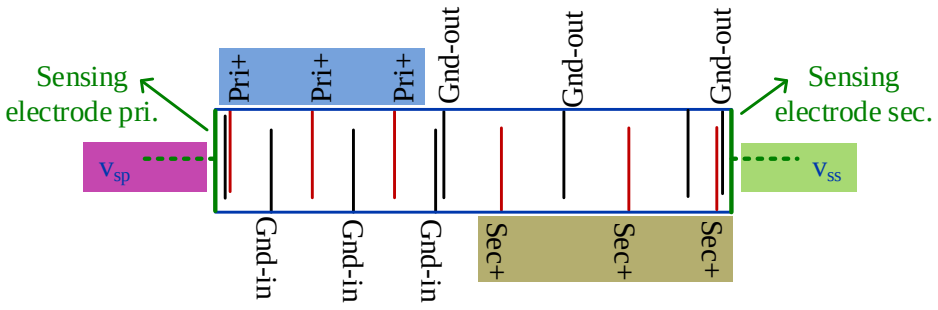


Figure 3.5: Measurement from sensing electrodes, first prototype.



(a) Prototype



(b) Layout

Figure 3.6: PT with sensing electrode, the second prototype.

purpose, but the PT itself did not have the native ZVS capability. However, PTs with feedback electrode are not used for the further experiments done is this work.

3.2 Improvement of self-oscillating loop

Employing PTs in a relatively narrow frequency range in which they exhibit inductive characteristic ensures providing current for the output capacitance of the switches to alternatively being charged and discharged for obtaining ZVS. This problem in the PT-based power converters is particularly addressed by applying a feedback loop operatively coupled between the sensing signal from the electrode of

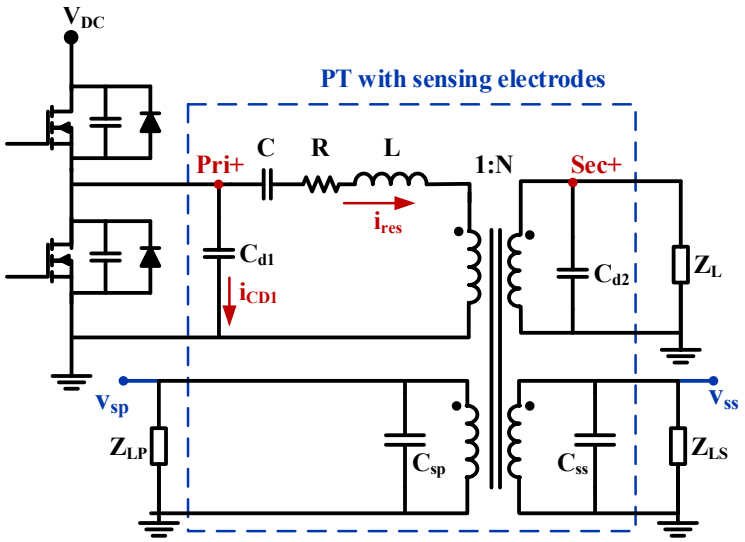


Figure 3.7: The equivalent circuit of PT with the sensing electrodes.

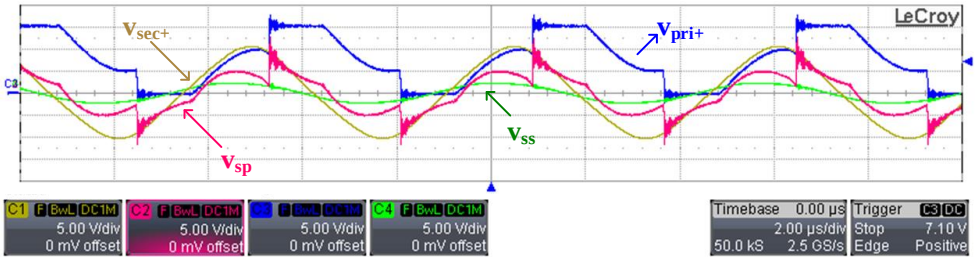


Figure 3.8: Measurement from sensing electrodes, the second prototype.

the PT and input to the gates of switches in order to provide a self-oscillating loop around the primary section of the PT [23]. Essentially, an analog self-oscillating loop results in fast tracking of changes in the PT's characteristic. However, analog design by itself has shortcoming in the previous research due to lack of resolution for dynamic tracking of PT's characteristics [18, 22, 23]. PTs are utilized within a narrow frequency span in which very small changes of phase shift in the self-oscillating loop reveals a considerable difference in the output voltage level. In order to overcome this shortcoming, a dynamic time delay is inserted in the loop followed by a control block shown in Fig. 3.9. A closed-loop phase shift self-oscillating is designed with a digital-to-analog converter (DAC) and a field-programmable gate array (FPGA) board. The resolution of the applied time delay in the new designed self-oscillating loop is 1 ns.

3.2.1 Design considerations

Fig. 3.10 shows a detailed drawing of timing signals. In the digitized delay line (DDL) block, the input signal DDL_{in} is the shifted zero crossing of the estimated

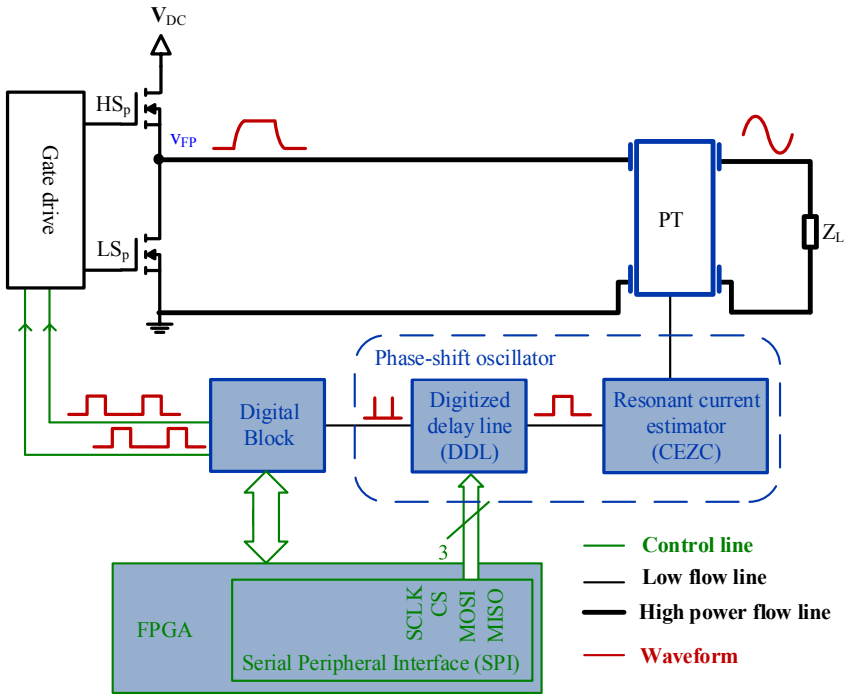


Figure 3.9: The modified self-oscillating loop with a digitized phase shift.

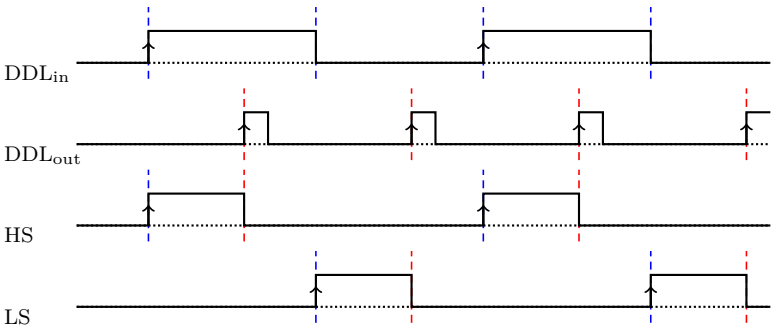


Figure 3.10: The input and output signal waveforms of the DDL and the DB blocks.

resonant current with 50% duty cycle. The output signal of the DDL block is a one-shot pulse which is the time-delayed version of the input signal. The amount of the delayed time is proportional to the output value of the DAC which is set by the interface made in LabVIEW software. In each cycle the high-side and low-side switches are turned on by rising edge of the input of the DDL block, DDL_{in}, and its negated, respectively. The output of the DDL block, DDL_{out}, indicates the turn off time of the switches. More details about the operating principle and experimental waveforms are provided in the Appendix D.

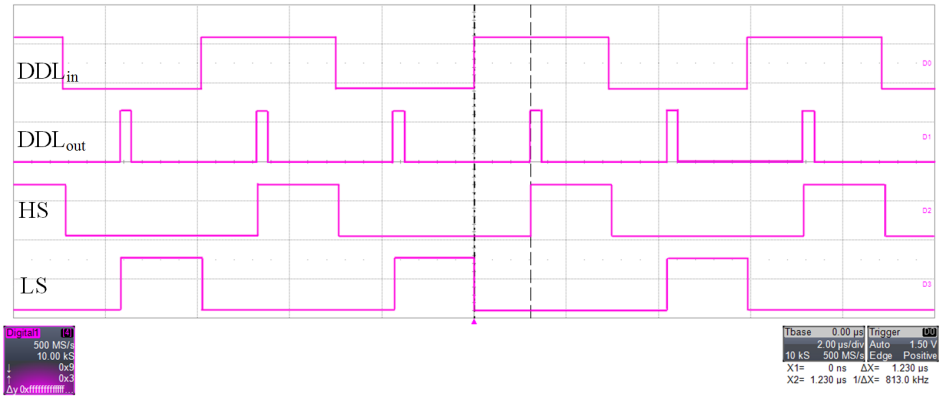


Figure 3.11: Measurement: input and output signal of DDL and control block.

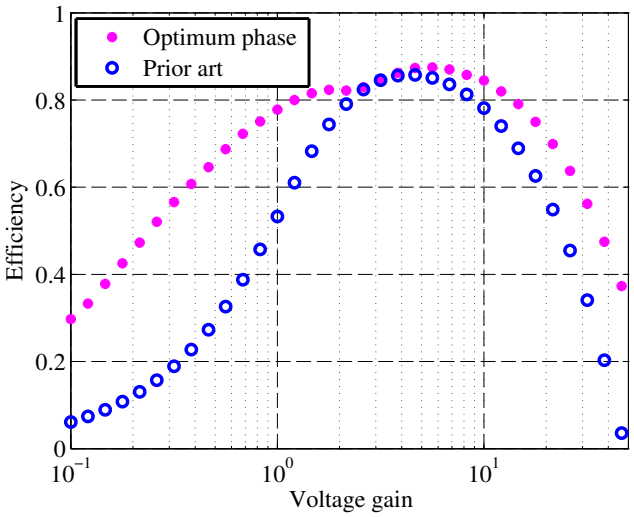


Figure 3.12: Efficiency improvemnt by implementing the optimum phase delays.

3.2.2 Experimental results

Fig. 3.11 shows input and output signals of the DDL block together with high-side gate voltage (HS) and low-side gate voltage (LS). Fig. 3.12 shows simulation result for maximum efficiency by implementing optimum phase delays. The prototype of DDL block diagram is built, shown in 3.15 and tested with the switching frequency of 118.3 kHz, which is related to the PT's operating point. Figs. 3.13 show efficiency measurement as a function of the voltage gain of the converter by sweeping the delay in DDL block. In order to achieve the maximum efficiency of the converter in each voltage gain, the related time delay can be detected and applied. Fig. 3.14 shows the interface for delay sweeping. Figure 3.15 shows two different boards used for the DDL block. The functionality of the designed board DDL is explained in the Appendix D. There is also found a commercially available integrated circuit (IC) with a resolution of 1ns time delay step that can replace the analog circuit of the DDL board. The test board is shown in Fig. 3.15. However, the analog circuit

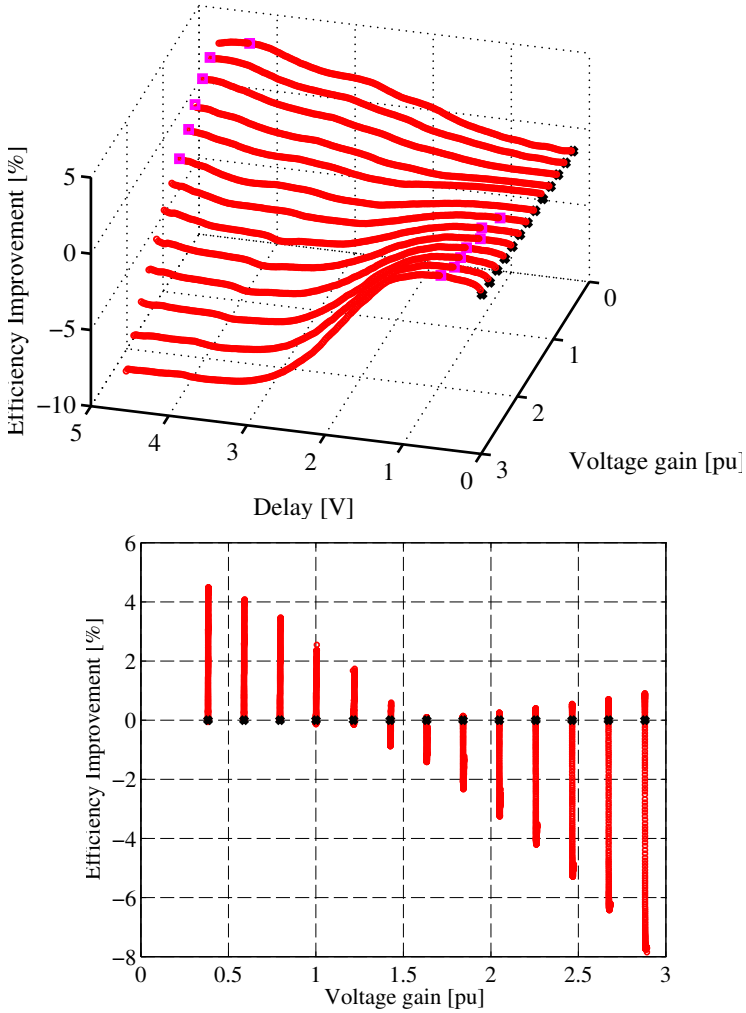


Figure 3.13: Measurement of efficiency as a function of the voltage gain with the sweep of time delay.

is more convenient for this application, since it is able to provide 1 ns time delay resolution in a broad range.

3.2.3 Summary

By applying very fine delay steps, efficiency increase can be achieved in the PT-based converters. This investigation has done by implementing digitized delay line to the self-oscillating loop for the PT-based SMPS. Applying digital steps to the loop is performed by a DDL block through a FPGA development board and a control interface. The results show that by imposing this new method, high efficiency can be attained in a wider span of the voltage gain compared to the previous research (Fig. 3.12). Notably, the applied control technique requires modification in order to be able to automatically select the optimum delay attributed to the maximum attainable efficiency.

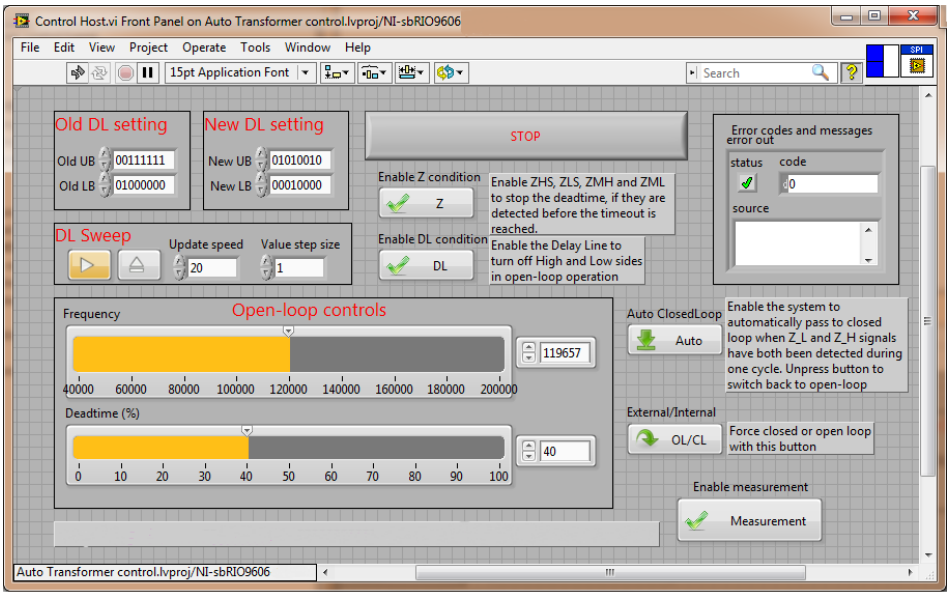


Figure 3.14: The LabVIEW interface used for digital control signals.

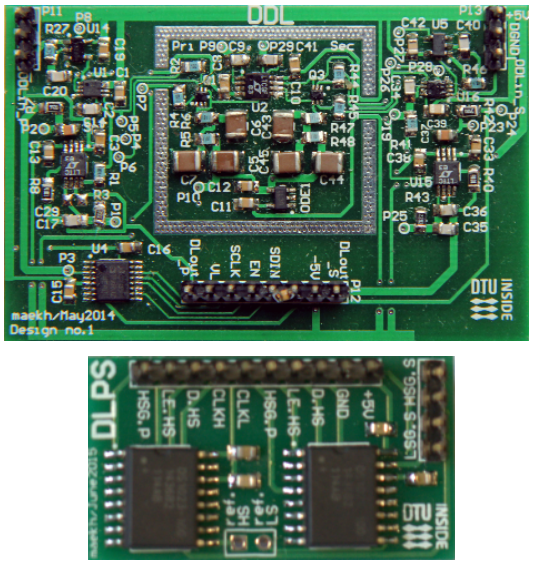


Figure 3.15: The DDL designed board, compared to the available IC.

3.3 Current sensor

It is important to measure the input current of the PT for control systems in the power converter [38]. The measured current can be used for different purposes. First and foremost, the input current to the PT is equal to the resonant current during the time span where switches are on. In the operating points for which ZVS is achieved, the resonant current changes its direction during the on time of the switches. Therefore, sensing the input current of the PT allows measuring the trend of the resonant current. Notably, there is typically no access to measure the resonant current directly from the PT. Tracking the phase of the current helps for the control techniques used for the PT-based SMPS, which in this research has been the phase shift control method. Furthermore, the amplitude of the sensed current is related to the amplitude of the resonant current, which is also useful for tracking the changes in the amplitude of the resonant current in the control system, for instance, for finding the operating points at which PT has a larger amplitude. This means that the PT can deliver larger current to the output. Moreover, sensing the current allows for dynamic measuring of the input power to the transformer during the operation.

An investigation and simulation showed that there will be more convenient to measure the input current of the PT from the high voltage line. Measuring current from the high voltage line in the presence of high input switching voltage is a difficult task since the switching voltage $v_F(t)$ has a transition from ground to the high voltage, in this application 200 V, in a very short period of dead time (DT). This transition occurs when the resonant current charges or discharges the input capacitance of the PT during DT. But in this application measurement of the resonant current during the on time of switches is of particular interest. The frequency bandwidth of the PT's operation is typically 300 kHz, for instance the operating frequency range of between 112 kHz to 120 kHz for the PT's used in this research. Moreover, the input current to the PT is an AC signal with positive and negative values which requires a bi-directional current sensor.

The most commonly used techniques for current sensing are resistive sensing and magnetic sensing [39, 40]. In this application, due to its usage inside the strong magnetic field, the magnetic sensing cannot be used. Moreover, the input current of the converter was not large in this case. Notably, the amplitude of the resonant current is imposed by the PT and its resonant frequency. This further adds more difficulty to sense the differential voltage across the sensing resistor. Moreover, the PT's operating frequency normally varies between 50 kHz to 300 kHz, which needs a current sensor with an effective bandwidth of more than 300 kHz. The commercially available current sensors with the voltage line of approximately 200 V can only be found with a narrow bandwidth below 100 kHz. Therefore, a solution is proposed to these limitations by a new circuit design. Fig. 3.16 shows the block diagram of the PT-based SMPS employing bi-directional, resistive current sensing.

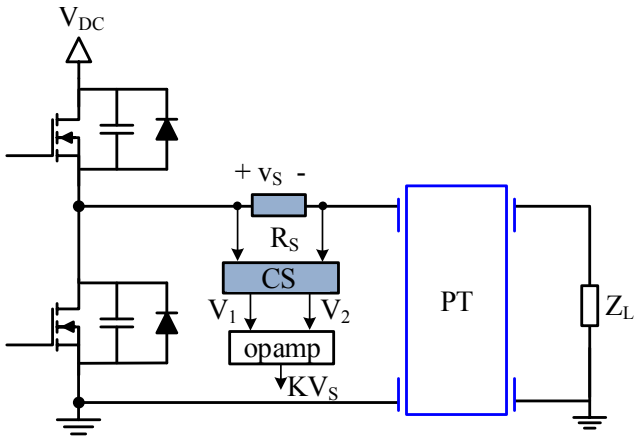


Figure 3.16: Current sensor for PT-based SMPS.

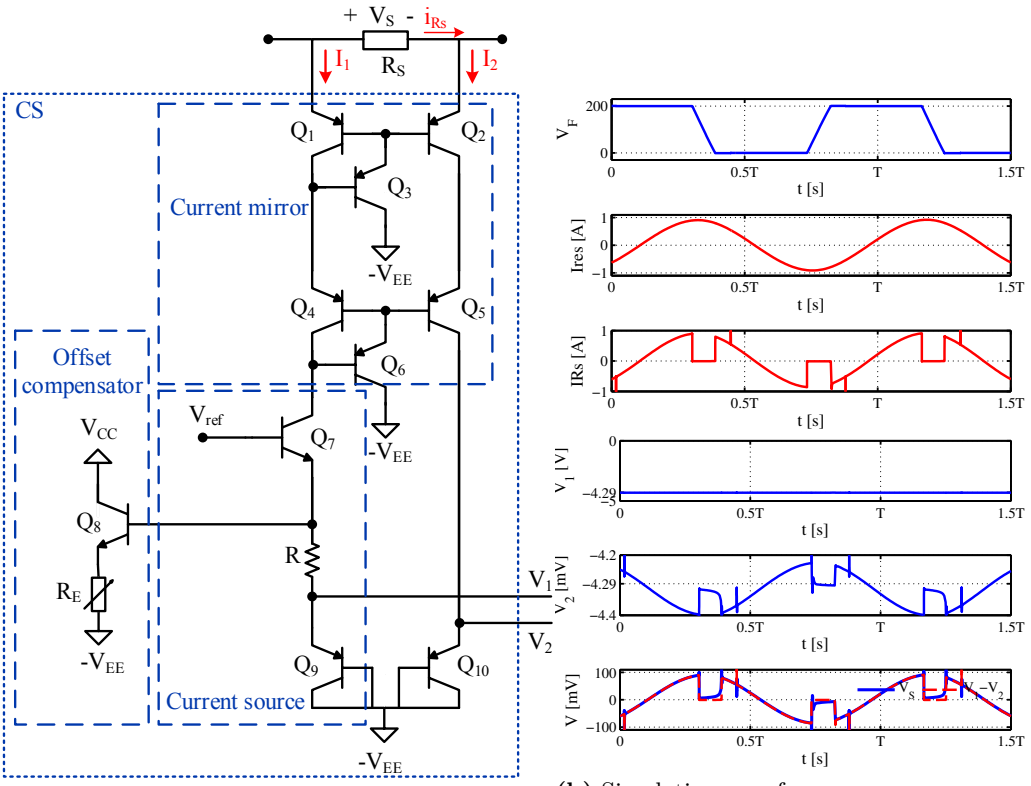
3.3.1 Design and results

A sense resistor is put in the high-side rail between the switching node and the primary-side of the PT [40]. Fig. 3.17(a) shows schematic of the proposed current sensor. The inputs of the sensor are tied to the sides of the sense resistor R_s. The current through the sense resistor is the same as the resonant current when the switches are on or even when the body diodes of the metal-oxide-semiconductor field-effect transistor (MOSFET)s are conducting. Voltage across the sense resistor is directly proportional to the resonant current in this period. The output voltage represents the current flowing through the sense resistor, R_s, by transferring current to the voltage V_s with an amplification factor of K. Fig. 3.17(b) shows functionality of the sensing circuit by simulation waveforms. The component in use and the values of parameters are provided in the Appendix E. It can be seen that the sensing voltage, which contains AC waveform directly proportional to the resonant current, has been transferred to the voltage V_2 and contains a DC offset. The value of this DC offset can be adjusted to the output voltage V_1. The voltage difference of V_1 and V_2, (V_1-V_2), will be the same as V_s and can be amplified through an op-amp. Details about the functionality of the circuit and design considerations can be found in the Appendix E

Fig. 3.18 shows the second built prototype. The PT in use cannot handle to transfer large amount of power, therefore the input voltage set to the low value i.e. 12 V. Thereby, the sensing voltage was very low in value and at the noise level. Moreover, the influence of the switching noise in this specific place of measurement, which is directly connected to the switching node, complicated the measurement.

3.3.2 Summary

A new circuit of a bi-directional, resistive current sensor is proposed. The designed sensor is particularly suitabel for functioning in the presence of a high common mode voltage, in this application 200 V, with a wide frequency bandwidth of several kHz, in this application 200 kHz. The sensor's tolerance for the common mode voltage and the frequency bandwidth depends on the selected components. The



(a) Schematic circuit

(b) Simulation waveforms.

Figure 3.17: Schematic circuit and simulation waveforms of the wide bandwidth, bi-directional current sensor, operating with the high common mode voltage.

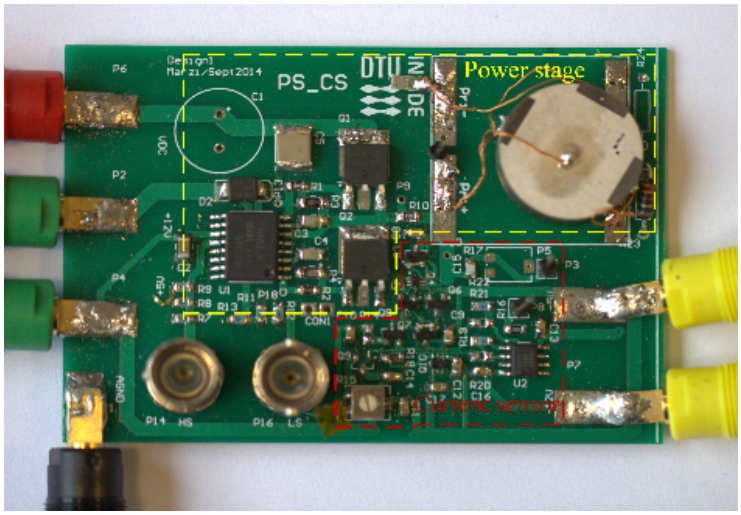


Figure 3.18: Prototype of the current sensor for PT-based SMPS.

proposed current sensor has general application, even though its functionality has been investigated for a PT-based SMPS. Final measurement could not be carried out due to the impact of switching noises while working with the low input voltage

due to the limitations in the PT. Therefore, more consideration for noise reduction should be considered which requires further work. Due to the scope of this project, further research could not practicably be carried out on this part.

3.4 Optimum dead time (ODT)

In the SMPS adequate DT is needed in order to attain soft switching [16], [41–43]. Since PTs are used for high voltage applications, ZVS as a type of soft switching is more beneficial for the PT-based SMPS due to decrease of switching losses. Moreover, sufficient DT is important in order to deliver proper energy to charge and discharge the input capacitance of the PT and ultimately, obtaining ZVS [14, 17,29,44]. This chapter explains an innovative method for detecting optimum dead time to attain ZVS. Fig. 3.19 shows simple block diagram of a PT-based converter with ODT block which imposes its output pulses to the digital block in order to turn on the switches.

3.4.1 State-of-the-art for the dead time

Obviously, in a SMPS there is a necessity of imposing an interval during the switching transition when both switched are turned off [42], [45–50]. This time interval, known as dead time, and prevents the current from shoot through. In a PT-based SMPS, the DT interval within which all switches are off, allows the resonant current to charge or discharge the input capacitor of the PT [14, 17]. Ultimately, making proper conditions for having ZVS [29] in the switches in order to decrease the switching losses [51–53]. This DT can generally be shorter or longer than required which in these cases hard switching may occurs [54]. Applying sufficient DT for the switches, results in soft switching which is ZVS in this case [41]. In

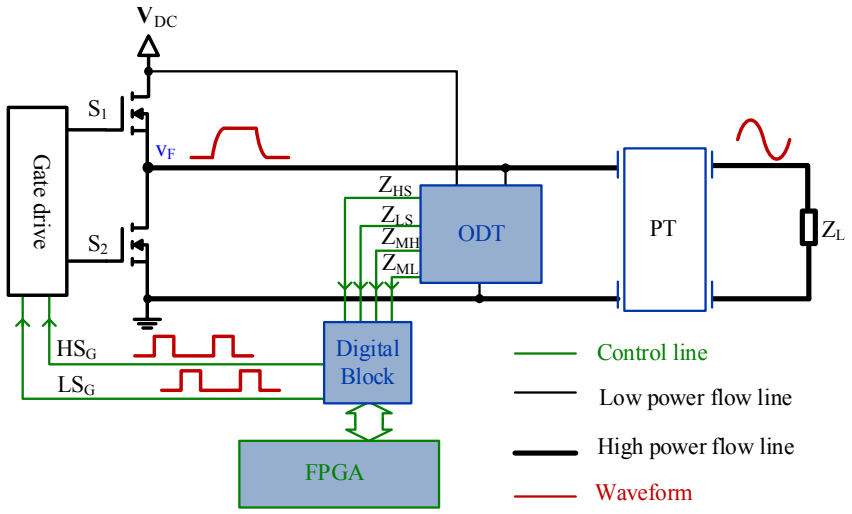


Figure 3.19: The block diagram of the PT-based SMPS with contribution of the ODT block which leads dynamic detection of the optimum DT in each resonant cycle.

the past research, the DT was taken to be a fixed value in order to ensure the achievement of ZVS in the steady state [18, 22, 24, 34]. The fixed value of DT was selected specifically for every PT and it was typically long for the steady state and for the initialization operations. Therefore, it took longer for the converter to reach the steady-state by imposing a long DT during the start-up time. The reduction of start-up time is more important in some applications when the converter needs to be frequently turned on and off, for example when burst-mode control is used. The proposed solution to this limitation is implemented successfully and turned to a filed patent application.

3.4.2 Design considerations

The idea of optimizing DT is implemented in this research. In this method of optimization the switching voltage $v_F(t)$ is scaled down to the level of the comparator's input. The rising edge of the output signals Z_{MH} and Z_{ML} will affect the gate signals during the initialization period or the steady state when the voltage across the input capacitor of the PT, $v_F(t)$, does not reach the positive or negative rails due to the low amplitude of the resonant current. The rising edge of the output signals Z_{HS} and Z_{LS} turn on the high-side, S1, and low-side, S2, switches when the switching voltage $v_F(t)$ reaches the positive and negative rails, respectively. The waveforms for these two cases are shown in Fig. 3.20.

However, for achieving ZVS the signals applied to the gates of the switches should be in a way that the switching voltage $v_F(t)$ leads the resonant current in the phase. Therefore, the time point at which low-side switch is turned off is taken as a reference point in the waveforms. More details about the control techniques and operation of switches under the ZVS condition are described in the Appendices H and F. Finally, the contribution of output signals of the ODT block together with the initial gate signals, which can be imposed externally or through the self-oscillating loop, is controlled by the digital block. Fig. 3.21 shows implementation method of the designed circuit. The detailed description of the circuit is provided in the Appendix F.

3.4.3 Result

Experimental results show successful detection of the optimized DT with the implemented method. Fig. 3.22 shows the results in the steady state when the ZVS is achieved and Fig. 3.23 shows detection of the ODT when the amplitude of the resonant current is not big enough to charge the input capacitor of the PT to the positive rail. More details about this cases are explained in the Appendix F. Furthermore, efficiency increase of the converter with the optimum DT in comparison with previous research [22], in which a fixed DT is used, is shown in Fig. 3.24. Fig. 3.25 shows the prototype of the ODT block. For the purpose of this research the ODT circuitry is designed in a modular board with the flexibility of being switched on or off from the control loop through enable signal. The size of the ODT block can easily be reduced for commercial products.

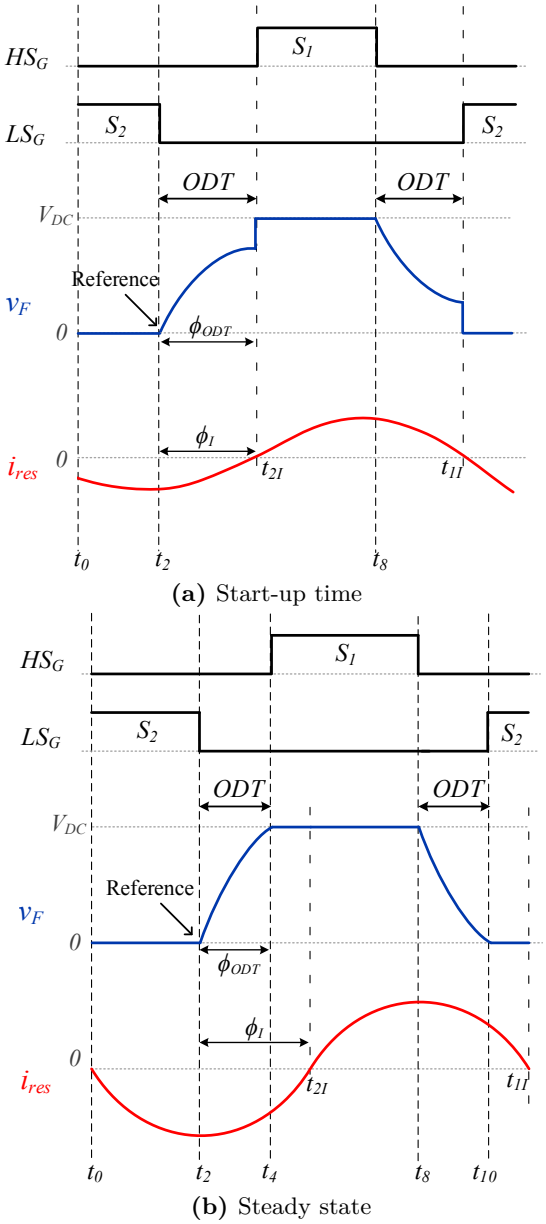


Figure 3.20: Waveforms after detection of the optimum DT.

3.4.4 Summary

A new method of optimizing the DT for SMPS is proposed and implemented in this research. A block circuit is designed in order to be added to the converter followed by a digital block for correction of the gate signals. The ODT block can be used for the gate signal correction when the gate signals are applied externally or through a closed-loop e.g. self-oscillating loop. Even though the ODT is particularly applied for inductorless PT-based SMPS in this work, the method can thoroughly be used for other resonant power converters. The ODT is used due to its effective build up of the resonant current in the start-up time through minimization of the DT and reduction of switching losses by allowing the ZVS during the steady

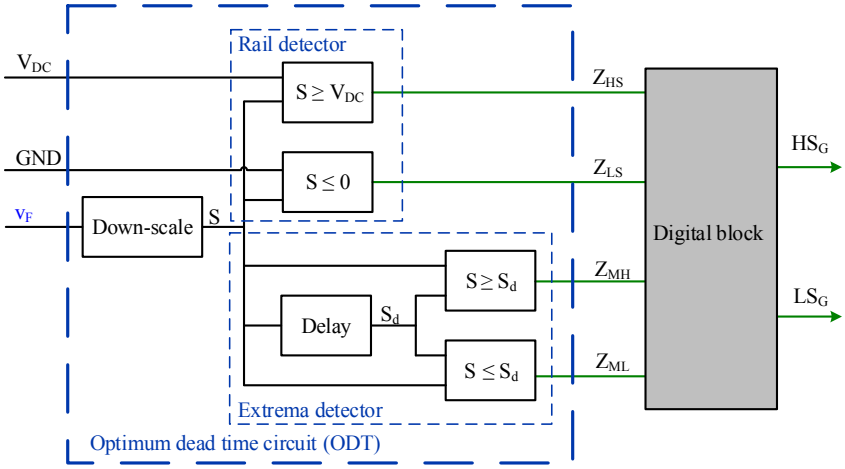


Figure 3.21: Desciption of the ODT circuit with simple block diagrams.

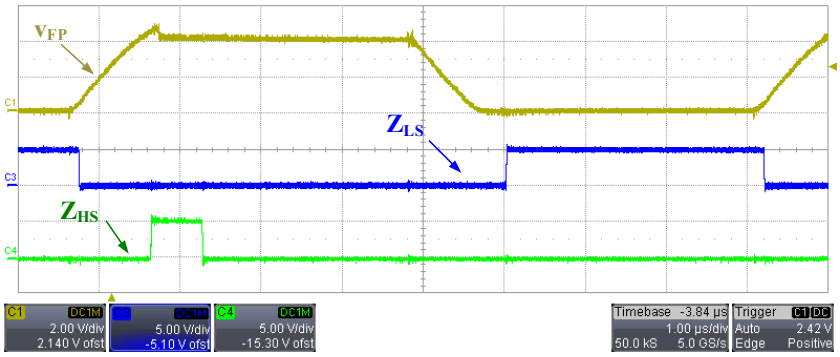


Figure 3.22: Experiment shows control signals Z_{LS} and Z_{HS} in the output of the ODT block.

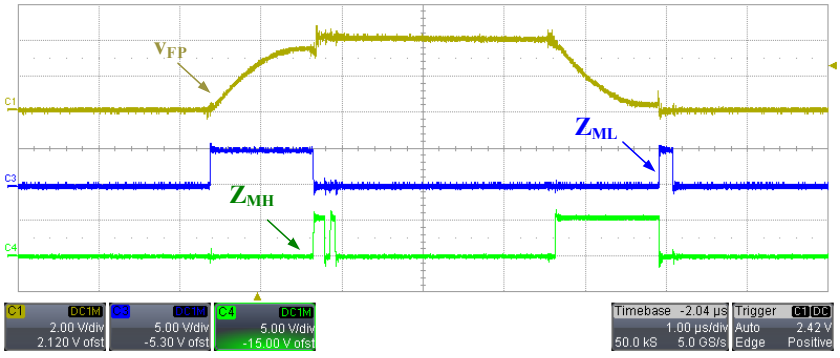


Figure 3.23: Experiment shows control signals Z_{ML} and Z_{MH} in the output of the ODT block.

state. The disadvantage of using the ODT is that it adds complexity to the control method. Moreover, the proposed method for detecting the ODT is filed as a patent application enclosed in the Appendix G.

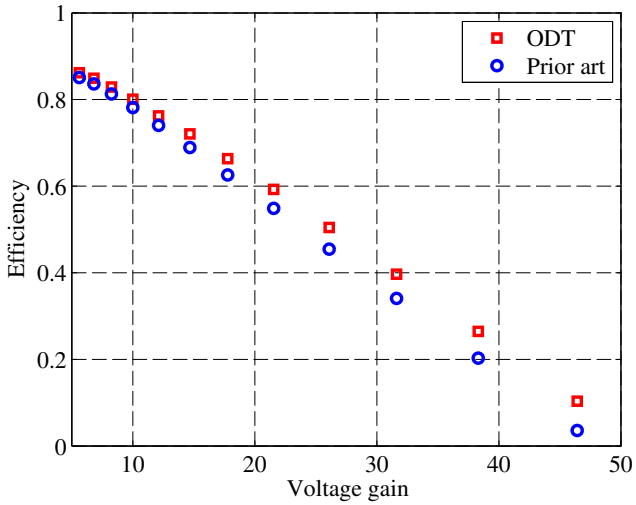


Figure 3.24: Simulation result showing efficiency improvement before and after the ODT detection.

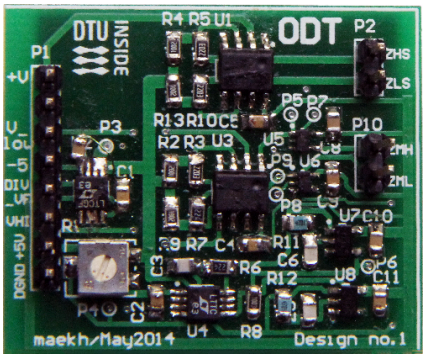


Figure 3.25: Prototype for the ODT block.

3.5 Summing-up of the unidirectionality

In this chapter unidirectional PT-based converter with resistive load and capacitive load has been tested. Fig. 3.26 shows the block diagram of a unidirectional PT-base SMPS. The functionality of the PT-based SMPS in its all operating modes is described in the Appendix F. Implementing the optimum phase and dynamic detection of ZVS by contribution of DDL and ODT blocks shows efficiency increase. Figure 3.27 shows efficiency comparison by adding each of the new blocks individually and also together with the self-oscillating loop.

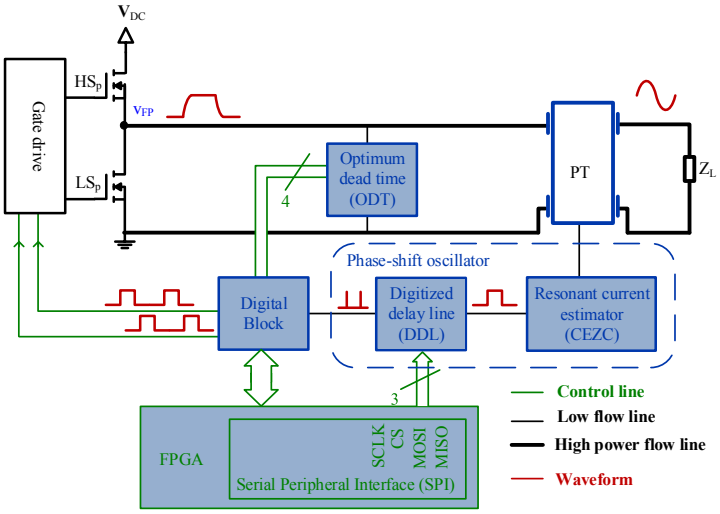


Figure 3.26: Block diagram of the unidirectional PT-based SMPS.

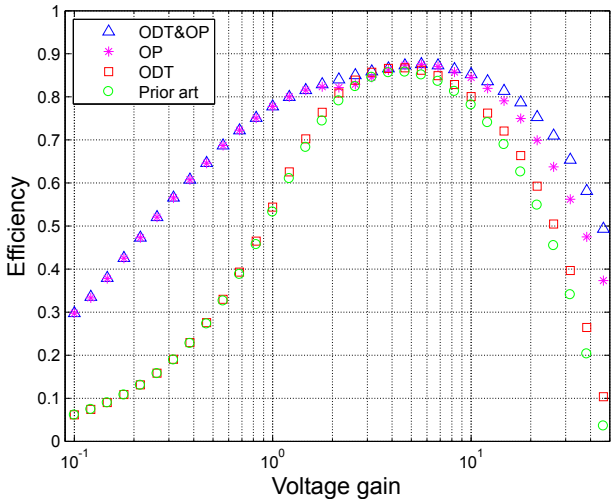


Figure 3.27: Efficiency improvement by adding the DDL and ODT blocks. Prior art: the previous research with a fixed DT; ODT: the ODT block is added to the converter; OP: the DDL block is added to the converter; ODTand OP: both ODT and DDL blocks are added to the converter.

Chapter 4

Bi-directional topology

In this chapter focus will be on applying control techniques employing energy recovery from the capacitive load i.e. piezo actuator. A thorough analysis of ZVS for the inductorless PT-based SMPS with the half-bridge topology is introduced. Furthermore, a new control method for controlling the operating point of the PT for the bi-directional topology is proposed. The proposed control technique is implemented in two different configurations. The experimental results for the applied techniques are provided.

4.1 Analysis

Generally, it is desirable to find a frequency range in the power converters for which the ZVS can be obtained [7, 28, 29]. In practice, obtaining ZVS for all of the switches in a bi-directional PT-based power converter is a difficult task. Therefore, a comprehensive analysis of ZVS region for the resonant converters and particularly for the PT-based SMPS with a resistive load, and a capacitive load with a passive or an active rectifier is provided in this section. Ultimately, the represented method can help in overcoming the limitations in the control technology of the SMPS and particularly PT-based drivers [26], [55–57].

The analysis is done by finding a simplified equivalent impedance seen from the switching nodes [58, 59]. Furthermore, this work gives an estimation on the value of the ODT under the soft switching condition. Fig. 4.1 shows overall waveforms for the inductorless PT-based SMPS. In general, in order to obtain the ZVS the gate voltages of the switches should allow the voltage $v_{FP}(t)$ leading and the voltage $v_{FS}(t)$ lagging the resonant current. In the waveforms in Fig. 4.1 the phase shift between the primary switching voltage, $v_{FP}(t)$, and the resonant current, $i_{res}(t)$, is ϕ and the phase shift between the secondary switching voltage, v_{FS}, and the resonant current is $\Delta\phi_S$. Therefore, by adjusting the phase shift between the primary and the secondary switches, which is $\phi+\Delta\phi_S$, the amount of the reverse power flow can be controlled. The proposed and implemented control technique is explained in the Section 4.2 of this Chapter.

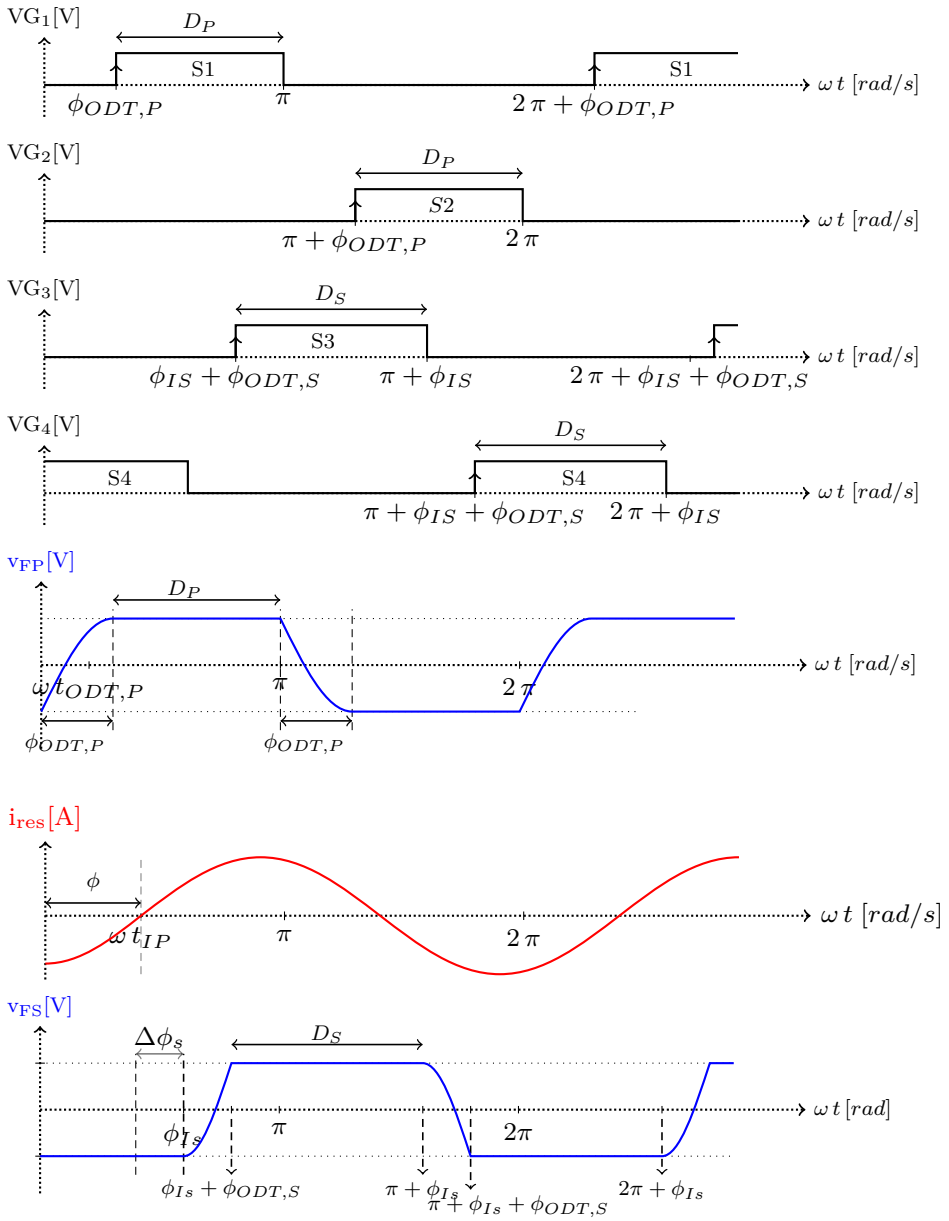
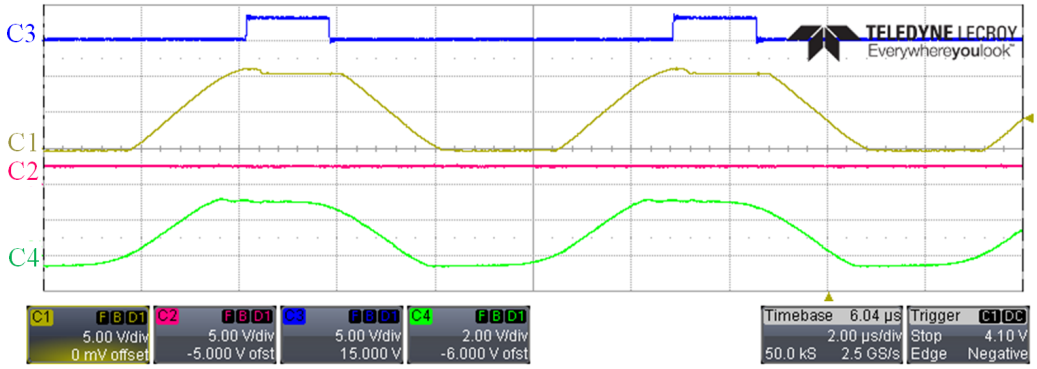
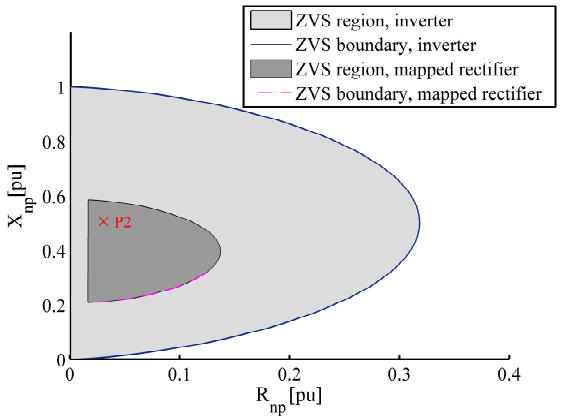


Figure 4.1: Waveforms in the bi-directional topology: Gate voltage of switches, resonant current i_{res} and switching voltages of the inverter $v_{FP}(t)$ and the rectifier $v_{FS}(t)$.

Investigations for different operating points with and without the ZVS achievement for the inverter and the rectifier networks are carried out in the Appendix H. The rectifier network is either passive or active, comprised of a diode rectifier or a switching network [60–62]. This analysis further finds the ZVS region for the inverter and the rectifier networks. Fig. 4.2(a) shows the switching waveforms for an operating point, P2, where the inverter's and the rectifier's switches have soft switching. Fig. 4.2(b) shows the mapping of the rectifier's ZVS region into the inverter's ZVS region for the same operating frequency of P2. The point P2 is well-situated in the overlapping area of the ZVS regions which is matching with the



(a) The operating point P2 for the PT-based converter with half-bridge diode rectifier with V_{in}=10 V, frequency=114.8 kHz, R_L=100 Ω, V_o=2.5 V. C1: Inverter's switching voltage v_{FP}; C2: Output voltage V_o; C3: Gate voltage of the S1; C4: Rectifier's switching voltage v_{FP}.



(b) The mapped rectifier's ZVS region for the switching frequency of 114.8 kHz.

Figure 4.2: ZVS regions of the rectifier and the inverter seen from the inverter's side.

waveforms shown in Fig. 4.2(a).

4.2 Control techniques

In order to control the energy recovery from a capacitive load, a phase shift should be applied between the primary and secondary switching networks [22, 25]. This phase shift control is implemented by a time delay inside the digitized self-oscillating loop. The implementation of the digitized control method for the self-oscillating loop is explained in the Section 3.2 of Chapter 3 as well as in the Appendix D.

Fig. 4.3 shows the first control implementation. In this method there is a complete isolation between the primary- and the secondary-side of the power converter. The primary and the secondary switches are driven by the gate voltages generated in

individual self-oscillating loops. Both loops use separate estimation of the resonant current where the delays are set by the optimum delay line (ODL) block for the related loops.

Fig. 4.4 shows the block diagram of the second implementation. In this method of control the control system uses one reference for the estimated resonant current. The frequency is locked through the primary loop and the ODL block in the secondary-side applies a phase shift to the secondary switches with reference to the primary switches.

The ODL block is composed of two sub-blocks ODL_{on} and ODL_{off}. The input of the ODL block named CEZC, is delayed by ODL_{on} to turn on the switches at its rising edge. The output of the ODL_{on} is tied to the ODL_{off} and imposes more delays to the ODL input signal in order to turn off the switches at the rising edge of its ouput pulses. The delay applied by the ODL_{off} defines the on time of the switches.

In both methods of implementation the digital block (DB) is controlling the final gate signals. Moreover, the digital commands for controlling the applied delays to the ODL and DB blocks are controlled by a FPGA through an interface shown in Fig. 4.6.

The implemented control systems have the same functionality. In the first implementation there is an isolation between the primary- and the secondary-side of the converter. This is beneficial for applications which requires full isolation. The PT's operation is more stable in the second implementation, since there is one estimated resonant current used for the reference. The stability of the resonant frequency is also highly dependent on the design of the transformer in use. Further isolation can easily be applied in the control system to gain the advantage of fully isolated converter. Moreover, the PT used in these implementations should have different ground in its primary and secondary sides to make the isolation possible.

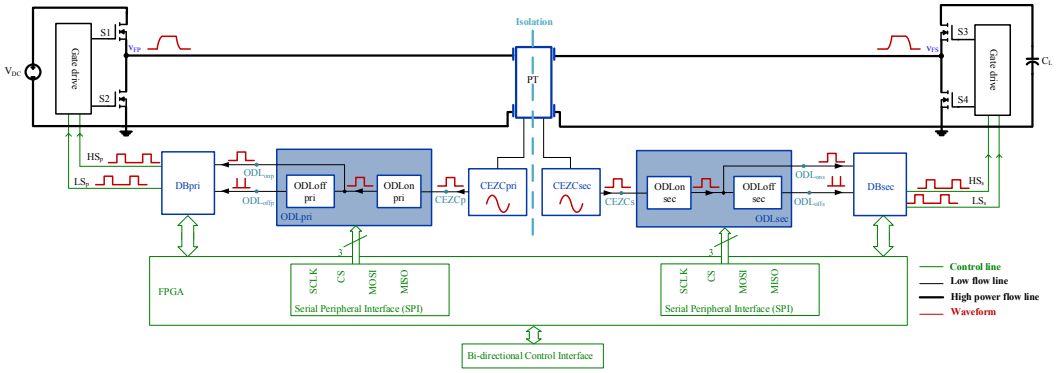


Figure 4.3: Bi-directional block diagram; the first implementation.

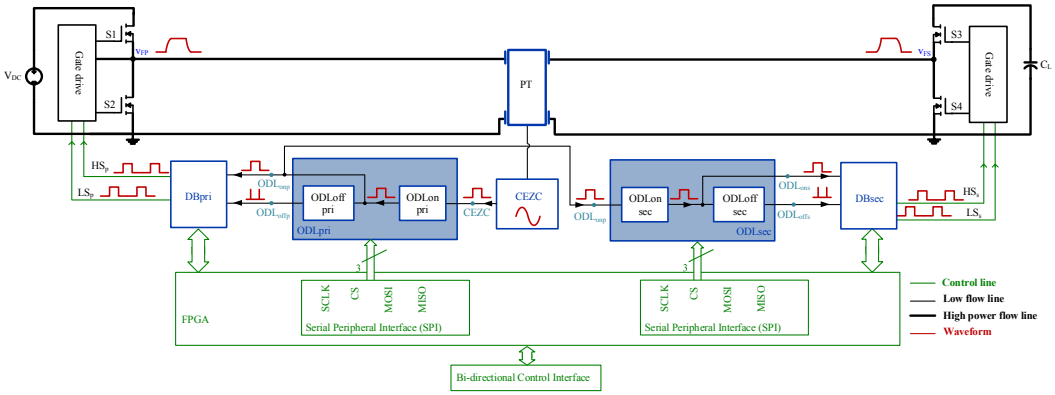


Figure 4.4: Bi-directional block diagram; the second implementation.

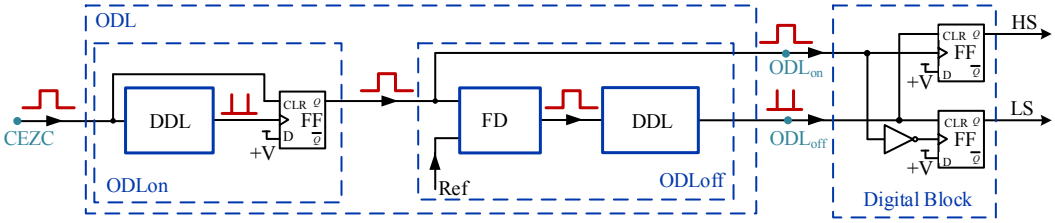


Figure 4.5: Bi-directional block diagram; the second implementation: ODL block.

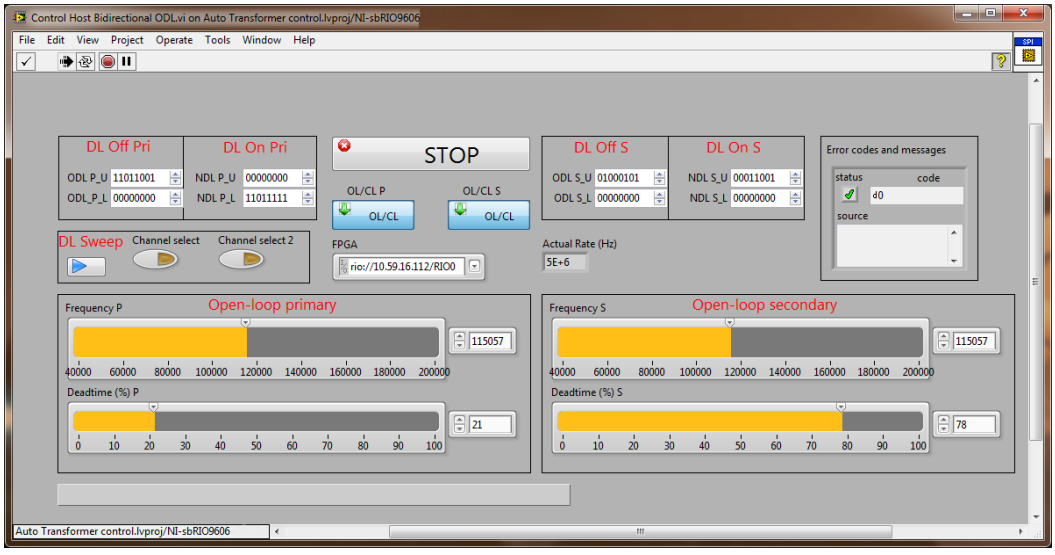


Figure 4.6: The bi-directional control interface.

4.3 Results

The designed circuits developed in the unidirectional topology described in the Chapter 3 are utilized for the bi-directional configuration as well. Additionally, the new control techniques are added for bi-directional functionality of the designed

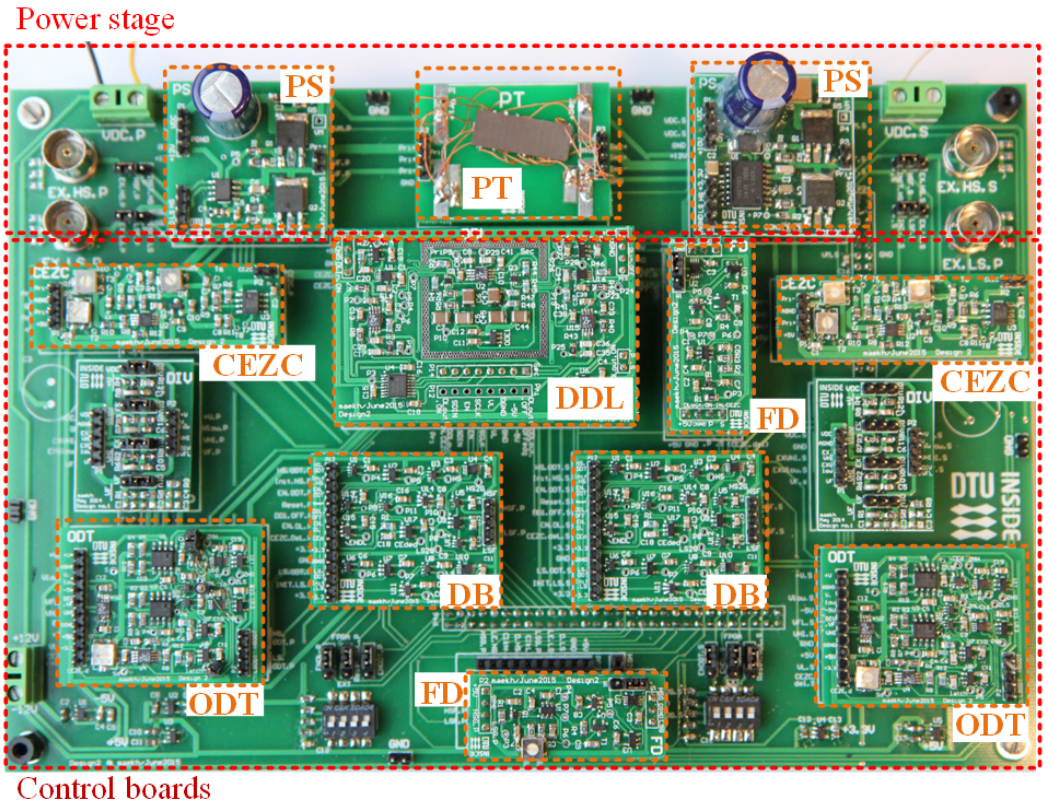


Figure 4.7: The project's second prototype; bi-directional board.

power supply. This shows electronic circuitry and the experimental results.

4.3.1 Final prototype

A prototype is built and tested with successful results through the implemented bi-directional control systems. Fig. 4.7 shows the prototype and Fig. 4.9 shows simple block diagram of the built prototype including all the modules designed during this research.

4.3.2 Experiments

Fig. 4.8 shows the experimental results. In this experiment the delays are set to achieve the ZVS for the primary and the secondary switches at the frequency of 115 kHz. The setting values in the control interface are shown in Fig. 4.6. The ZVS is attained in all switches by fine adjustment of delays and phase shifts through ODL blocks and the optimum dead time is detected by the ODT block.

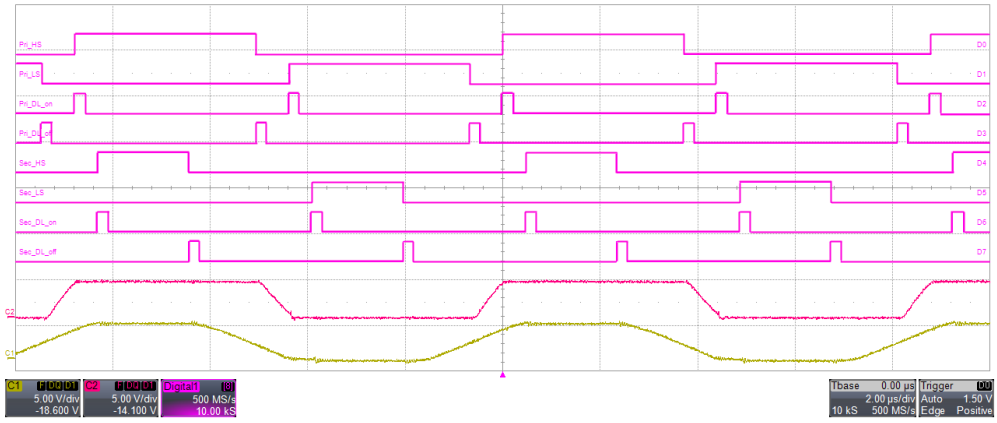


Figure 4.8: Experimental waveforms.

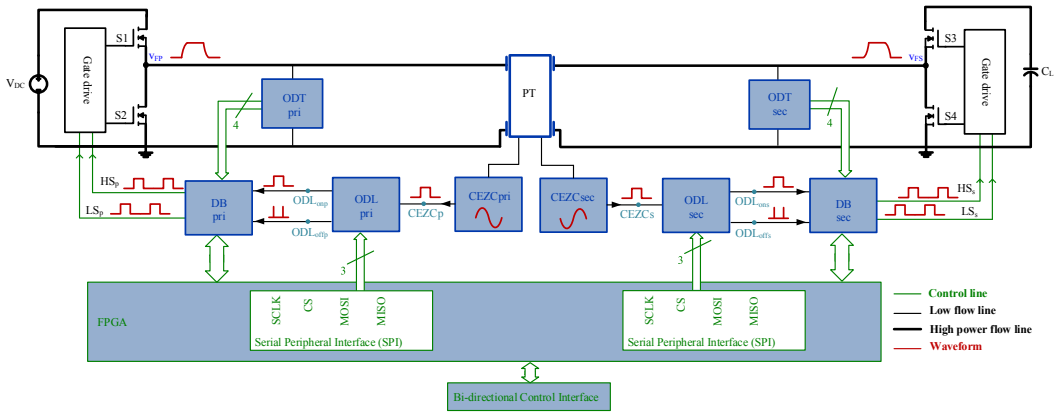


Figure 4.9: A simple block diagram of the bi-directional configuration.

4.4 Summary

The ZVS analysis carried out in this chapter can be used as a guideline to predict the optimum operating point of the SMPS for obtaining ZVS by proposing a ZVS region for the switching networks. This analysis can be generalized for all types of resonant converters, even though the discussion focuses on the inductorless PT-based SMPS. A new control system is designed and implemented to investigate the bi-directional functionality of the power converter through the phase shift control method. The proposed method applies very fine time delay steps to follow changes in the PT characteristic and to find the optimum operating point for the structure of the entire converter in terms of soft switching and efficiency.

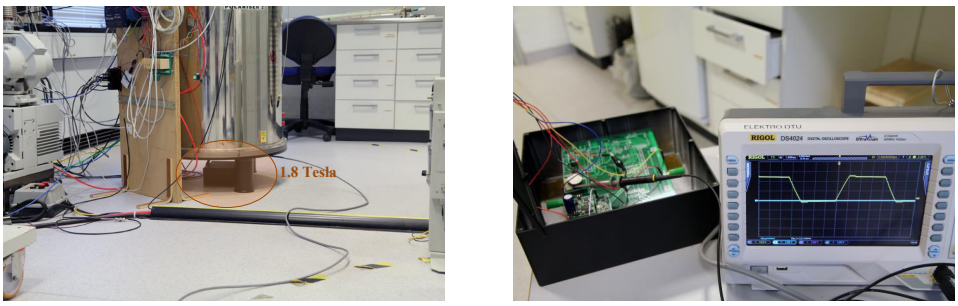
Chapter 5

Test of the driver inside the strong magnetic field

MRI is a test that uses a magnetic field and pulses of radio wave energy to make pictures of organs and structures inside the body. Therefore, it is very important that equipments used inside the room e.g. motors and electronic circuits are compatible with related medical standards. The goal of this project was to design a nonmagnetic driver which can be integrated inside the housing of the PAD motor or can be placed under the patient's table. For this reason no magnetic component i.e. inductor and magnetic transformer used for the converter.

5.1 Test in the magnetic field

The first test was performed in the magnetic field laboratory at the Technical University of Denmark. Figure 5.1 shows the test setup where EMI enclosure containing the driver was located under the magnetic field bore. The location provided the strongest and a uniform magnetic field measured of 1.8 Tesla.



(a) Setup in the magnetic field laboratory. **(b)** The prototype circuit in the EMI enclosure.

Figure 5.1: Test in the laboratory magnetic field.

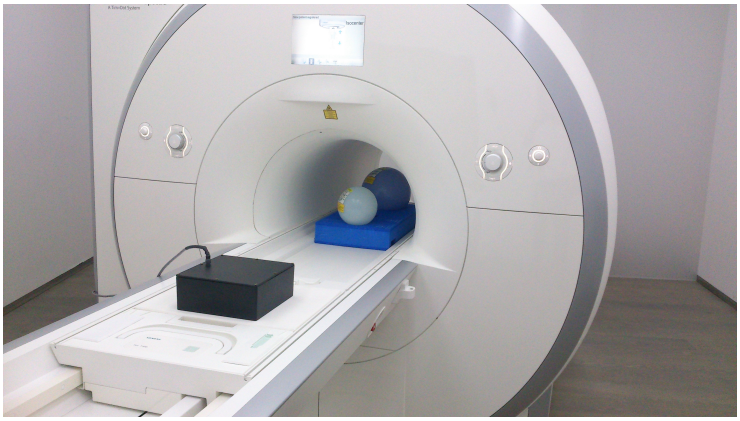


Figure 5.2: Setup inside the MRI chamber with the EMI enclosure and the test circuit.

5.2 MRI test

Two phantoms used to evaluate the electronic circuit inside the 3 Tesla magnetic field. One field with oil and another field with water. 3D digital images from an MRI scan were stored for more study on a computer in the MRI operating room. The nominal resonance frequency in the volume of the oil phantom was 125.25 MHz at 3 Tesla. Fig. 5.2 shows the test setup inside the MRI chamber. The driver circuit was located on the MRI patient table with the distance of 40 cm from the entrance of magnet bore and an imaging phantom, with diameter of 24 cm, and filled with special oil.

The power supply providing the input DC voltage and the auxiliary voltages to the PT-based SMPS were located outside of the MRI chamber in the control room. The cable connection between the power supply and the enclosure box was made via a shielding penetration with a Siemens connector filter. The enclosure box containing the driver circuit was placed at 40 cm from the phantom. Figure 5.3 shows the complete test setup.

5.3 Measurement of electromagnetic stray radiation

In order to detect any disturbing stray radiation at fixed frequencies, relevant frequency spectrum for MRI was scanned with the antennas inside the magnet bore. During the test the converter's switching frequency was 119 kHz and the control clock was 80 MHz. The measurement span was approximately 9 minutes, during which no fixed frequency components stand out in the radio frequency (RF) spectrum. There was no observation of interference from neither the switching frequency nor the control clock. The study of RF image from the computer in operating room showed that the overall signal to noise ratio of the imaging system was reduced by approximately 10 dB. This was attributed to a suboptimal choice of enclosure and large physical size of the driver and the FPGA boards used. Figure 5.4 shows impact of the driver setup on the image in terms of RF noise.

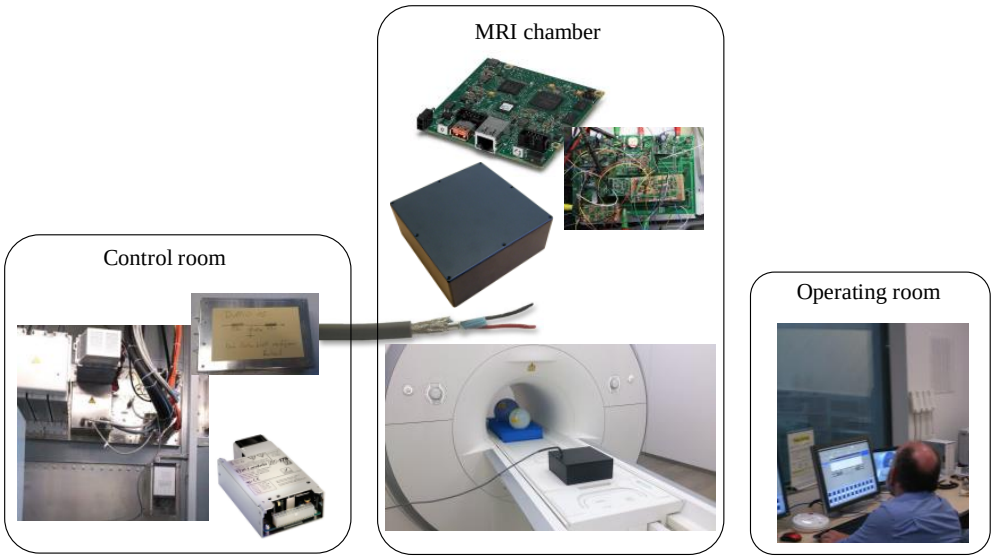


Figure 5.3: The whole test setup for the MRI test.

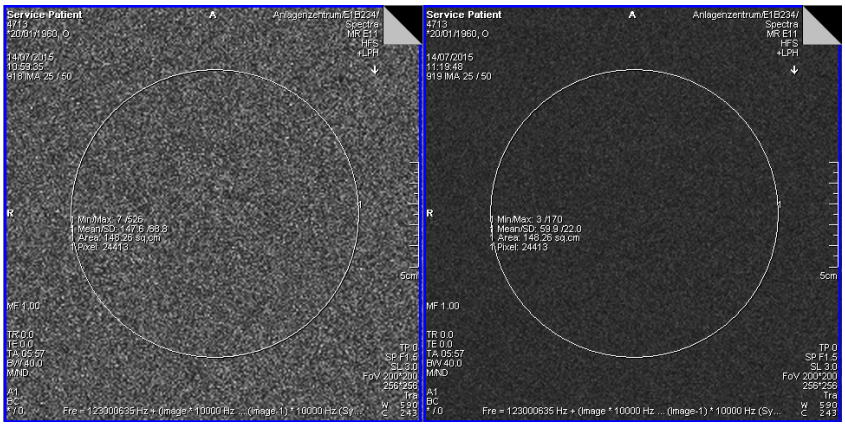


Figure 5.4: The RF analysis with and without the driver's circuit inside the EMI enclosure.

Moreover, impact of the magnetic field on the performance of the driver was tested which showed full functionality during the test.

5.4 Effect of eddy current on the conductive parts

Due to the alternating magnetic gradient fields during the imaging process, eddy current effects were caused inside any conductive materials in the magnet bore. Effect of eddy current on the enclosure box was sensible only inside the magnet

bore when the box was kept between hands. The level was well below the inherent eddy current effects of the MRI system itself. An improvement can be obtained by better EMI enclosure.

5.5 Summary

There was no outstanding observation of EMI from the electronic circuit of driver to the MRI imaging. The driver had full functionality under the strong magnetic field. From electrical point of view it has been a successful research along with the initial aim of the project. This means that imaging and driver operation can occur simultaneously, which results in more effective medical imaging, to the benefit of patient. This further shows that the approach of utilizing piezo transformers, and avoiding to use any magnetic component was a right decision and should be continued for similar types of applications.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

The work presented in this thesis and the associated publications addressed many facts of the overall problems in working with the PT-based SMPS with the goal of increasing efficiency. The outcome of the investigation performed during this research are integrated to the major and sub-contributions. As the major contributions:

- An improvement performed in the self-oscillating loop. In order to follow variations in the output voltage of the PT, a very fine time delay resolution of 1 ns in the self-oscillating loop was required. The important key was to have 1 ns resolution in a relatively wide range of phase shift inside the self-oscillating loop. The commercial available ICs were not able to cover the demanded span of phase shift with minimum 1 ns resolution. Therefore, a digitized delay line circuit was designed with the combination of analog and digital techniques. Each step of time delay inside the phase shift self-oscillation loop results in a very fine change in the resonant frequency of the PT. By this implemented method, the optimum value of delay can be detected in terms of efficiency. The work done in this research dealt with the implementation of the idea and sweeping the delay times in order to measure the efficiency. Selection of the optimum delay was done manually. Further research is required for dynamic detection of the maximum efficiency point, automatically.

- Minimum dead time for switching the MOSFETs in a PT-based SMPS is introduced and implemented. This implementation is filled as a patent application. The optimum DT is implemented in a ODT block in order to sense the switching voltage and turn on the switches when it reaches to the rails. Dynamically detecting of the ODT decreases the switching losses. Moreover, it leads the converter for faster reaching the steady state which is more beneficial when burst mode control is applied.

- The detailed analysis of the ZVS conditions and regions for the PT-based

SMPS is performed in this research. It is important that all the switches obtain the ZVS in a single operating point. The introduced analysis helps on finding a common region that all switches obtain soft switching. The method is generalized for similar type of resonant converters. The analytical method has shortcoming in defining the ZVS region that can be easily implied to the experiment. This is firstly, because of unpredictable changes of the PT's operating point in terms of temperature variations. Secondly, it is because of complexity of analytical methods due to correlation of related parameters.

- A new method for implementing bi-directional PT-based SMPS was proposed. The new block circuit of the ODT and the ODL blocks are well-utilized for controlling the self-oscillating loops, and for obtaining the ZVS in all the switches, from almost fully forward to the almost fully reverse power flow. The prototype was built with modular sub-circuits to give flexibility to the research purpose. The final prototype can be very compact with integrated control techniques inside the FPGA and reduce the analog circuits. Principle of the bi-directionality is implemented, but further research is required for adding an outer control loop, in order to control the output voltage with the maximum efficiency and generating a 200 Hz sinusoidal voltage.

- A new circuit is proposed for sensing the input current of the PT which is partly equal to the resonant current. Sensing the current simplifies the control techniques and reduces the size of the control system. The circuit showed intended functionality, but further research is required to reduce noises in the designed board for a clear measurement for the existing PT's with power transferring limitations.

  As the sub-contributions:

- The methods for power enhancement of the PT is implemented. Three different samples of PTs are fabricated. The measurement result showed that the designs were not successful as expected due to the production limitations. Furthermore, two prototypes of PTs with an auxiliary tap were designed and fabricated in order to sense the resonant current inside the transformer. Experimental results showed a step forward to the goal, but the produced PTs cannot be used in the converter's prototype. In the first prototype, the amplitude of the sensed signal was at the noise level, therefore, the resonant current cannot be recognized properly. In the second prototype, previous issue resolved by increasing the thickness of the piezo layer used for giving feedback from the resonance, but unfortunately PT was not able to inherently achieve the ZVS. In fact, the idea of sensing the resonant current through an auxiliary tab will be promising by a new deign. The advantage of having a sensorless detection of the resonant current is reduction of the size of control system by eliminating the CEZC block, as well as complexity reduction in the control techniques.

- Successful demonstration of unaffected SMPS performance and MRI imaging quality carried out through testing the prototype in a Siemens Magnetom Vision MRI treatment table. The designed converter tested inside the MRI room in order to measure the interaction between a high magnetic field and the electronic circuit. The driver had fully functionality inside the MRI scanner

room. There was observation of RF noise from electronic circuits to MRI images. Investigation showed that the reason for RF noises were improper enclosure box used for shielding the converter. For future tests, a better compatible enclosure box can improve the impact of final PAD driver package on the MRI room. This requires an expensive enclosure box which can be provided for the test of the commercial products.

6.2 Perspectives on future research

The width of the covered topic resulted in significant improvements in the soft switching, control techniques, efficiency and performance of the PT-based SMPS. As a further research there are number of topics which are addressed as follows:

- Driving a piezo actuator demands for a piezo transformer with capability of transferring about 100 watts without dramatic temperature increase. This requirement puts strict demand on the design and fabrication of a PT with low loss, high power density and ZVS factor with the value of close or more than one for the primary- and the secondary-side of the PT.
- Further research needs to be performed on the design and fabrication of a PT with auxiliary tap for sensing the resonant current. This will significantly reduces the size and complexity of the control system.
- A minor modification is required for the digital delay block. Adding a control strategy to the DDL block, makes it possible for the converter to automatically select the optimum delay or the phase shift related to the maximum efficiency.
- The proposed combination of the digital and analog techniques can be further extended to improve the energy efficiency of the converter by detecting the optimized switching frequency in terms of the efficient operating point of the PT.
- In order to reduce measurement noises in the current sensor circuit, a new PCB board should be designed. Including the current sensor to the converter would ease the control strategy and reduces the size of the control system.
- Further investigation of the proposed bi-directional control techniques needs to be carried out. It is important to control the energy recovery from the load in order to deliver the required power to the capacitive load and keep the output voltage to the desired level.
- If the future applications still demand for four piezo actuators, placed inside the PAD motor, to be provided by reactive power whilst being driven by sinusoidal signals with amplitude of 200 V, offset of 100 V and phase shift of 90 degree, then further research needs to be carried out to accomplish this aim.
- Special research needs to be carried out to design the outer loop for generating a sinusoidal voltage with frequency of 200 Hz to drive the piezo stacks placed inside the PAD motor. For the PT-based power converter with a narrow

frequency bandwidth, an advanced control concept needs to be implied in order to generate an AC signal in the output over a wide range of voltage levels.

- In the future, applications demand that the control system be integrated inside the housing of the PAD motor. This aim requires miniaturization of the electronics in order to provide a compact driver board for commercial products. The digitized control system performed in this research brings the possibility of integrating the control techniques inside the processors i.e. FPGA. Additionally, a new electronic board should be designed utilizing tiny packages of the components for the analog part of the system. This will be possible due to the existing available components. However, further research needs to be carried out to accomplish this goal.

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Appendix A

Nonmagnetic driver for piezoelectric actuators

Presented at

IEEE International Conference on Electronics Circuits and Systems (ICECS 2014)

Nonmagnetic driver for piezoelectric actuators

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***Abstract*—Piezoelectric actuator drive aims to enable reliable motor performance in strong magnetic fields for magnetic resonance imaging and computed tomography treatment tables. There are technical limitations in operation of these motors and drive systems related to magnetic interference. Piezoelectric actuator drive is the only form-fit continuous drive solution currently available for the development of high performance nonmagnetic motors. In this research focus will be on the non magnetic compact high efficiency driver for the piezo actuators and on employing energy recovery from the capacitive actuators. Therefore, piezoelectric transformer-based power converters are used for driving piezoelectric actuator drive motor in the presence of high electromagnetic field.**

Keywords — PAD motor; switch mode power supply; piezoelectric actuator; piezoelectric transformer

I. Introduction

Piezoelectric actuator drive (PAD) demands the use of piezo actuators for converting electrical to mechanical power and producing precise rotary motion. PAD characteristics, i.e. high speed independent torque, integrated force and position feedback allow for better performance and higher flexibility in the construction of treatment tables. This results in more effective medical imaging, to the benefit of patient. There are some limitations in the current treatment tables e.g. motors cannot operate in the presence of strong magnetic field inside magnetic resonance imaging (MRI) room. Furthermore, imaging and motor operation cannot take place simultaneously. Piezoelectric transformers (PTs) are suitable candidate for addressing this challenge. Development within PT-based switch mode power supplies (SMPS) has been increasing due to their smaller size, lighter weight, lower cost, lower electromagnetic interference (EMI), higher power density, and higher efficiency compared to magnetic transformers. Considerable efficiency increase by achieving soft switching in PT-based SMPS has been reported [1]. In total, using PAD motors and PT-based SMPS will have clear cost advantages. This project aims on creation of compact and high efficiency driver which allows for bi-directional current flow together with employing control methods for stabilization of PTs operation.

II. PT- based SMPS

Inductorless SMPS based on PTs are used to replace conventional transformers in high power density converters. PTs allow converters to operate in high switching frequencies and by obtaining soft switching condition, switching losses will decrease. The operating principle of PT is based on electromechanical energy conversion. There is electromechanical coupling between the primary and secondary sides inside PTs, where the primary acts as a piezoelectric actuator and the secondary acts as a piezoelectric transducer. Providing adequate dead time in order to deliver sufficient energy for charging and discharging the input capacitance of PTs is required for achieving ZVS. This means that design of PTs and driving circuits must be performed together in order to ensure ZVS. Closed loop control is indispensable for compensating influence of parameters such as frequency and temperature, in order to have stable operation of PT and consequently accurate performance of the converter.

III. Challenges

PTs use electromechanical coupling between the primary and secondary sides compared to conventional transformers that use electromagnetic coupling. This introduces PTs as applicable candidates for applications which have a high sensitivity to electromagnetic interference, e.g. MRI scanners. Therefore, PT-based drivers will be able to work in high electromagnetic fields, e.g. 7 Tesla. One of the main challenges for PT-based power drivers is energy recovery through bi-directional current flow. This imposes strict requirements on the driver design. The driver should allow for suitable control of the PT, and techniques for obtaining high efficiency and compact converters. This arises need for new solutions which is of the interest of this research. Challenges in this work specifically are in three parts:

PT:
- · Raising power transmission capability of PT.

Power stage:
- · Obtaining high efficiency for driver.
- · Ensuring soft switching (ZVS).
- · Recovering energy through bi-directional functionality of driver.

Control: Implementing control methods
- · for stabilization of PT optimum operating point.
- · between primary and secondary MOSFETs for having bi-directional power flow to drive piezo actuator.
- · for providing sinusoidal voltage in the output of driver in order to drive PAD motor.

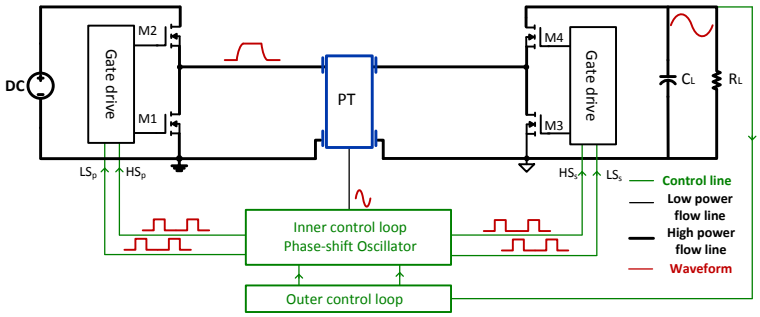

Fig. 1: Block diagram of power converter.

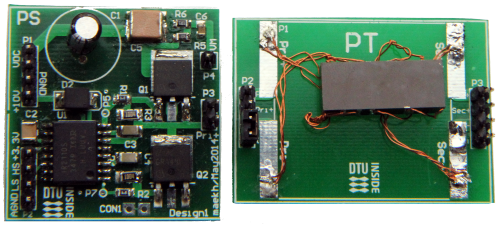

Fig. 2: Power stage (PS) and piezoelectric transformer (PT) boards used in the prototype.

IV. Methodology

Design of driver with the functionality of bi-directional current/power flow requires advanced control schemes to allow precise control of the capacitive load. An outer feedback is required for generation of a sinusoidal waveform to the PAD motor, in order to control the output waveform of driver with reference signal. Furthermore, for better performance of PTs an inner control loop is required to stabilize operation of transformer with correlation between PT's efficiency, temperature and frequency. PTs need to de designed carefully in order to have inherent ZVS characteristic and be able to transfer required power. According to the prior art, inductor-less half-bridge topology [1] and the self-oscillating control loop based on the phase shift is selected for resolving this challenge.

V. Research Project

A. State of research

Fig. 1 shows circuit block diagram of power converter and control structure have been considered in this work. Double feedback loop needs to be implemented in PT based DC/DC driver. One loop using phase control method for frequency adjusting to obtain ZVS and maximum gain/efficiency, and the other loop for output regulation. Temperature and load fluctuations cause changes in the operating point of PTs. A rise in temperature causes a decrease of resonant frequency. Therefore, a driver could easily shift out of the ZVS region or lead to a lower output voltage and efficiency. As a consequence, an inner closed loop control is important for maintaining PT operation at optimum point and desirable efficiency of driver. Presently, closed loop control is being performed by measuring phase difference between resonant current and switching signal. The purpose is adjusting switching frequency to the optimum value in order to ensure ZVS and obtaining maximum possible efficiency of PTs. Inductorless half-bridge topology has been employed as a power converter. Converter has been designed and built together with advanced control of self-oscillating loop based on both digital and analog control methods. The considerations for bi-directionality has been performed in design and built prototype. Fig. 2 shows power stage board and PT which are used as part of main board.

B. Further research

Additional control methods are added into the scope of this research to control bi-directional power flow. Bi-directional converters are targeted in this research but most work have been done on uni-directional converters. Further work is needed for investigation and implementation of control strategy between primary and secondary switch pairs.

VI. Conclusion

Piezoelectric ceramics are characterized as smart materials with widely applications. There are challenges in design of PTs e.g. increasing their power transmission capability and ensuring inherent ZVS. Furthermore, utilization of PTs in the power converters imposes strict requirements on the driver design. This demands for more complex control loops which requires further research. This project deals with employing control methods for designing compact and high efficient power supply with utilization of piezoelectric transformers.

VII. Acknowledgment

This project is supervised by Prof. Michael A. E. Andersen and Dr. Zhe Zhang in the Electronics group, at the Department of Electrical Engineering, Technical University of Denmark (DTU).

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Appendix B

State-of-the-art piezoelectric transformer-based switch mode power supplies

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Presented at

Industrial Electronics Society (IECON 2014)

State-of-the-art piezoelectric transformer-based switch mode power supplies

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***Abstract*— Inductorless switch mode power supplies based on piezoelectric transformers are used to replace conventional transformers in high power density switch mode power supplies. Even though piezoelectric-based converters exhibit a high degree of nonlinearity, it is desirable to use piezoelectric transformers due to their smaller size, lighter weight, lower electromagnetic interference, higher power density, higher efficiency, and lower cost. Moreover, PTs allow converters to operate in high switching frequencies and by obtaining soft switching condition, switching losses will decrease. This paper discusses power supplies with the trend evaluation of piezoelectric transformer-based converter topologies and control methods. The challenges of piezoelectric transformers regarding soft switching capability and nonlinearity are addressed. This paper can be used as a guideline for choosing a proper topology of piezoelectric-based switch mode power supply and a control method for the required application.**

Keywords—Piezoelectric transformer; Half-bridge topology; Bi-directional control method; Zero voltage switching

I. INTRODUCTION

Development within piezoelectric transformer (PT)-based switch mode power supplies (SMPS) has been increasing with regards to smaller size, lighter weight, lower cost, lower electromagnetic interference (EMI), higher power density, and higher efficiency. Furthermore, the manufacturing process of PT can be simpler than electromagnetic transformers, since any winding or core assembling are not required. The objective of this research is to summarize applied converter (specifically SMPS) topologies, employed control methods, reduction of switching losses and challenges due to the stabilization of PT's operation.

This paper explores PT-based converters and topologies that have been proposed for different applications. The primary focus of this paper is to review the topologies and control methods in PT-based SMPS. The study starts with a brief explanation of PT behavior in SMPS by its constraints and requirements. Thereafter, investigation has been conducted on the essentials of zero voltage switching (ZVS) in these type of converters and attempts to define ZVS regions or factors for gaining desired performance of PTs inside the circuit. Comparison has been made between converter topologies together with the trend of their applications.

Examination was done on control methods used for increasing performance of converters by introducing the necessity of closed loop control. Closed loop control is indispensable for compensating influence of parameters such as frequency and temperature, in order to have stable operation of PT and consequently accurate performance of the converter. Bi-directional converters are targeted in this paper but most prior art used uni-directional converters; therefore, additional control methods were added into the scope. The control methods reviewed include: phase shift control, self-oscillating, burst mode and double feedback loop, etc.

The paper is organized as follows. In section II the state-of-the-art piezoelectric transformer-based SMPS is reviewed in terms of principles of PTs, their soft switching ability, uni-directional converter topologies, and control methods. In Section III, new challenges in the area of PT-based SMPS will be introduced. These are considered to be starting points for further research. Finally, conclusion is presented in section IV.

II. PRIOR ART

A. PTs in SMPS

Employment of PTs has become popular since it can replace magnetic and reactive components in both resonant and traditional magnetic transformer based converters. The switching frequency may be either above or below the resonant frequency of a PT. PTs can behave as inductors in a limited range above each resonant frequency. Furthermore, when PTs are operated slightly above resonant frequency, the series resonant network becomes inductive and provides sufficient resonating energy for charging its input capacitor. This results in achieving ZVS. Therefore, PTs can be replacements of resonant circuits in power converters.

The operating principle of the PT is based on electromechanical energy conversion. There is electromechanical coupling between the primary and secondary

This work is funded by "The Danish National Advanced Technology Foundation" with collaboration of Noliac A/S, Siemens Healthcare and IPU as partners.

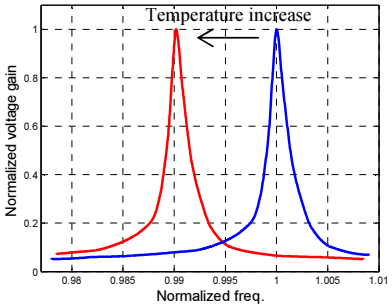

Fig. 1. Gain curve before and after a frequency shift from increase in temperature.

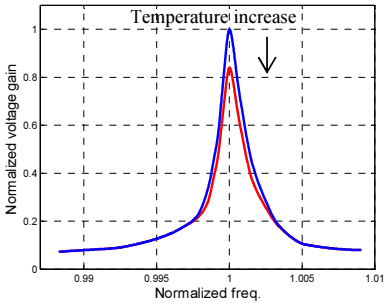

Fig. 2. Gain curve before and after an increase in loss resistance from an increase in temperature.

sides inside PTs, where the primary acts as a piezoelectric actuator and the secondary acts as a piezoelectric transducer. Transmitted energy ratio in PTs cannot exceed 95% due to piezoelectric material losses [1]. PTs are frequency-, load- and temperature- dependent [2, 3, 4, 5]. This fact influences their voltage gain and efficiency. Figs. 1 and 2 retrieved from [5] show variations of voltage gain due to temperature increment. Conclusively, a positive temperature change can result in both decrease of the PT gain and shift in its resonant frequency.

Some relationships between key parameters of PTs have been shown by generic closed-form equations [2], which can be used as analytical trade-off for design optimization of PTs in a required application. However, there are several production related parameters, e.g. size, oven temperature, polarization and electrode material, which bring some challenges to PT design. Furthermore, utilization of finite element method (FEM) software, e.g. COMSOL, gives a degree of freedom in PT designs for more considerations regarding application and fabrication [6].

PTs could be driven by either sine wave or square wave, while less reactive components are required for generating square wave [7]. PTs behave like high Q band pass filters; therefore they filter the input square waveform to generate sine wave resonant current and output voltage, which is mainly considered as fundamental signal of the input square wave. However, higher order resonant signals are also generated in the circuit which affects performance of the converter [8, 9].

B. Soft Switching operation and constraints

PT-based converters could benefit from soft switching due to significantly diminishing switching losses and stresses. Otherwise, energy stored in the input capacitor of PTs would be dissipated in MOSFETs and would cause hard switching. Researches show considerable increase of efficiency by achieving soft switching, e.g. efficiency has been increased from 70% to 83% by soft switching [10].

Providing adequate dead time in order to deliver sufficient energy for charging and discharging the input capacitance of PTs is required for achieving ZVS [11], besides preventing shoot through. This means that the design of PTs and driving circuits must be performed together in order to ensure ZVS.

Several attempts have been made to analyze the inherent soft switching capability of PTs by estimating [12] and providing analytical model for calculating [13] the load and the frequency boundaries. The obtainable ZVS region of PTs is very small regarding load and frequency [13]. Moreover, maximum obtainable soft switching has been derived in a simple relation [14] in order to design PTs under the matched load condition. This expression relates ZVS to the input and output capacitors of PTs in addition to efficiency (1). The equation demonstrates validating functionality of ZVS, with the design parameter of V_p' which is known as the ZVS factor.

$$V_p' = (0.304\ \frac{1}{n^2}\frac{C_{d2}}{C_{d1}} + 0.538)(0.585\eta + 0.414) \quad (1)$$

Where C_{d1} and C_{d2} are input and output electrode capacitances of PT, $n = \frac{1}{N}$ is effective turn ratio of PT shown in Fig. 5, and η is PT efficiency.

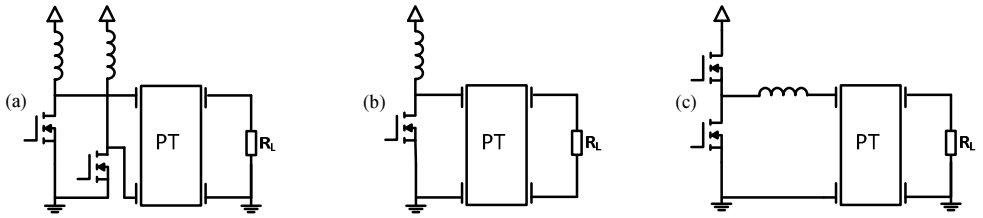

Fig. 3. Most popular converter topologies for driving PT: (a) Push-pull topology, (b) Class-E, (c) Half-bridge.

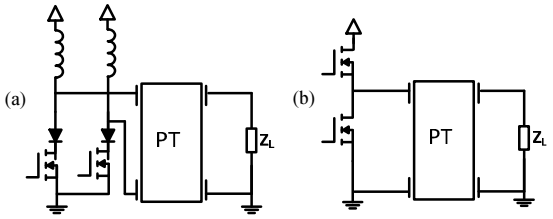

Fig. 4. Typical topologies for driving PT. (a) Current-source resonant inverter. (b) Voltage-source resonant inverter.

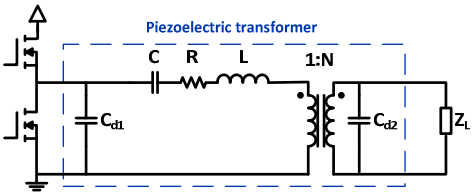

Fig. 5. Schematic diagram of the inductorless half-bridge topology and the Mason's lumped parameter model of PT.

C. *Uni-directional converter topologies*

As one of the initial researches on converter topologies, the dissertation [8] compares the performance of three different topologies of PT converters: half-bridge, single-ended multi-resonant (SE-MR) and single-ended quasi-resonant (SE-QR) PT converters. The comparison shows that DC/AC voltage gain for half-bridge and SE-MR can feasibly be below unity, while it is naturally above unity for SE-QR. Therefore, SE-MR and half-bridge can be used in step-down applications. The SE-QR is suitable for step-up applications and cost effective by having one switch and one inductor. Although half-bridge topology has more complicated structure and components than other alternatives, it has the advantage of greater efficiency and less generated noise.

Several standard topologies, i.e. push-pull, half-bridge and class-E, are investigated in [7, 15, 16, 17, 18]. Fig. 3 shows the most popular topologies for PT-based converters.

Push-pull topology has been recommended for step-up applications compared to half-bridge for reasons of simpler control and higher step-up ratio [7, 9]. Resonant push-pull drivers have been applied for continuous energy transferring with amplitude modulation for the first time [15] with a rough efficiency of 70%. The design benefits from two additional inductors. Compared to half-bridge topology, push-pull topology has less dissipation loss generated within the PT due to less filtration of input voltage harmonics [15]; therefore, there are more spurious modes in the resonant current and consequently output voltage.

Class-E and half-bridge topologies both are appropriate for step-down applications. Comparison of PT-based resonant topologies for step-down applications is performed [19], which result in priority for implementation of class-E compared to half-bridge due to better EMI suppression, lower switch current peaks, and larger control bandwidth. On the contrary, half-bridge topology shows better performance in high power levels compared to class-E [9, 19].

Some topologies have been identified as using PTs in parallel or series resonance for high-voltage power supplies [4]. Current source inverters have been used for supplying PTs in parallel resonance. The advantages to this are having less switching losses and voltage spikes compared to magnetic transformers, while the disadvantages are having unsatisfactory cost and size as a result of using two inductors for input current filtrations. Half-bridge topology has been utilized for the resonating of PTs around series resonance which leads to simpler and cheaper drivers. In both cases, PTs have been supplied by square wave form. Despite input current or voltage driving method, PTs behave as a voltage supply for the load. Fig. 4 shows these two types of topologies.

Nevertheless, there have been some prior efforts by utilizing one or several magnetic devices, i.e. inductors, for achieving ZVS in converters [8, 15, 20, 21]. The usage of one or more magnetic devices has been done in resonant converters by placing an inductor in series with a PT in the half-bridge topology in order to pump sufficient current into the input capacitor of the PT during dead time. With these approaches, full advantage of PTs could not be achieved and resulted in extra expense, size and effect of EMI in power supplies. Therefore, PTs should be used with inductorless converters in order to have effective reduction of cost and size [3, 12, 22].

Inductorless PT-based resonant converter topologies were analyzed for both AC output and DC output forms regarding obtaining ZVS [23]. Five different topologies were appraised for standard PT equivalent circuit. That research shows that in case of having optional dead time and frequency, achieving ZVS will depend on parameters, i.e. load condition, inverse of efficiency at the load condition and PT capacitor ratio. Finally, this resulted in ZVS-achievable criteria by standard equivalent circuit which is valid for any type of PT.

A method based on bootstrap method has been proposed in [24] for summation of several PT sub-converter outputs as a solution for non-isolated converters. Fig. 5 shows a block diagram of inductorless half-bridge PT driver.

Inductorless half-bridge topology has been employed for first ballast circuits with high efficiency and cost effectiveness for driving linear fluorescent lamp by utilization of radial vibration mode PTs [25]. In [14], this topology has been applied and a simple expression of soft switching capability has been revealed by empirical deriving of the ZVS factor. However, the shortcoming is that this factor is valid only when the load is matched.

D. *Control methods*

Temperature and load fluctuations cause changes in the operating point of PTs. Temperature increase is inevitable due

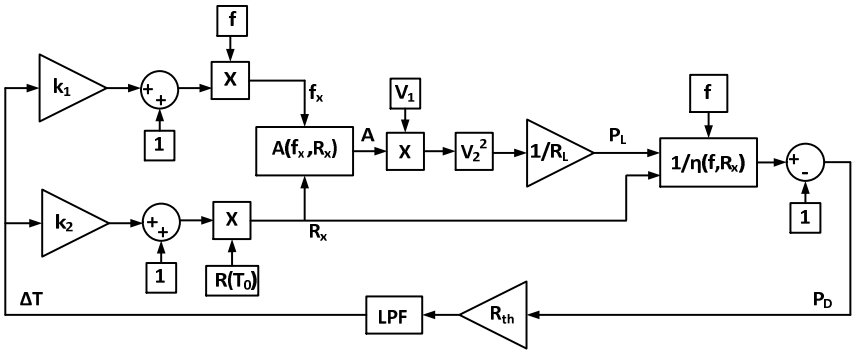

Fig. 6 Thermo-electric model of a PT with the effect of self-heating. Fitted parameters from measurements: K_1, K_2: constant and R_{th}: absolute thermal resistance to surroundings. f: applied frequency, V_1 and V_2 input and output voltages f_x: shifted frequency, R_x: temperature dependent loss resistor, R_L: load resistance, $A(f_x, R_x)$: temperature dependent gain, T_0: ambient temperature, ΔT: temperature change.

to power losses, while conversely there will be a decrease of mechanical quality factor in the PT, which turns into self-heating [5, 26]. Moreover, a rise in the temperature causes a decrease of resonant frequency. Therefore, a driver could easily shift out of the ZVS region or lead to a lower output voltage and efficiency. A valuable thermo-electric model has been provided in [5] and demonstrates nonlinearities. Fig. 6 shows a block diagram representing this thermo-electric model.

Several attempts have been made to apply control methods for PT-based converters. PTs exhibit a considerably narrow operating frequency range regarding their high quality factor, which brings challenges for obtaining soft switching and appreciable efficiency. However, keeping operating frequency in a proper point which is slightly above resonant frequency is hard to achieve by open loop. As a consequence, closed loop control is vital for maintaining PT operation at optimum point and desirable efficiency of drivers.

Presently, closed loop controls are being performed by measuring phase difference between resonant current and switching signal for the purpose of adjusting the switching frequency to the optimum value to ensure ZVS and achieve maximum possible efficiency of PTs [4, 27]. Closed loop control strategies allowing ZVS operation of converter have been suggested in [27, 28, 29]. Self-oscillating controls have been used in PT-based converters [30, 31] besides extensively using them in class-D amplifiers [32, 33, 34] as well as in DC-DC converters [35]. Self-oscillating control loops are used for the first time in inductorless topology on top of soft switching PTs in [36]; this shows the concept of beneficial utilization of self-oscillating loops in burst-mode controls, which are also known as quantum-mode controls since they have fast response in tracking resonant frequency at startup.

PT-based half-bridge drivers were used in [37] by utilizing burst mode control technology which has brought a 14% efficiency increase compared to the magnetic transformer-

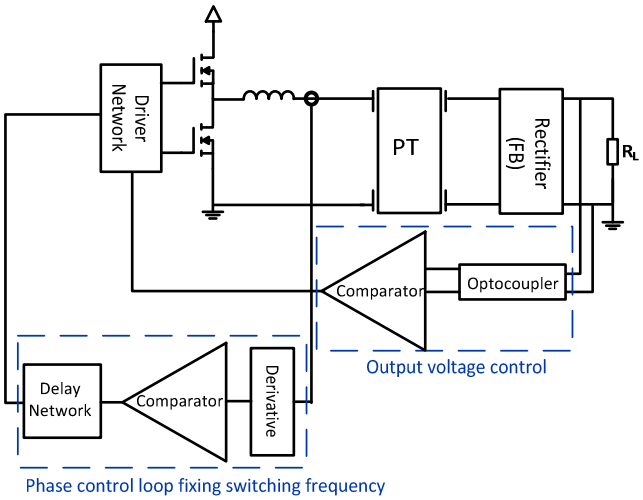

Figure 7: Topology with two feedback loops: resonant current phase and voltage control.

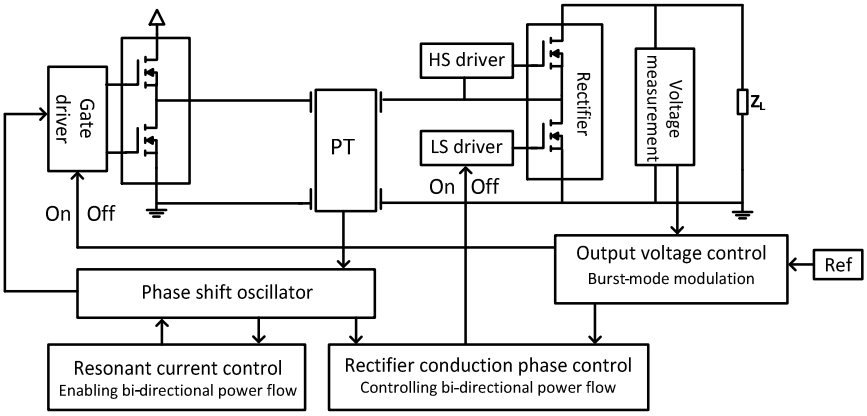

Fig. 8. Function block diagram of the bi-directional control method.

based counterparts. Additionally, it has been demonstrated that 41% loss reduction has been achieved plus considerable improvement in EMI in the frequency range of above 1MHz.

Double feedback loops have been implemented in PT-based DC/DC drivers [21]. One loop using the phase control method for frequency adjusting to obtain ZVS and maximum gain / efficiency, and the other loop for output regulation. With this proposed method, output voltage can be reached quickly. The block diagram of the driver is shown in Fig.7. The topology applied uses an inductor.

An inductorless driver has been implemented in [38] by taking advantage of previous double-closed loops with the combination of burst mode control technology.

E. Bi-directional control method

Bi-directional PT-based power converters have been implemented for dielectric electro active polymers (DEAP) actuator as load [11, 39]. Phase shift controls were employed in order to avoid the use of two different PTs for achieving ZVS in both forward and reverse energy flow. Experiments substantiate the claim of bi-directional power converters with active phase shift controls and utilization of just one PT. Fig.8 shows a block diagram of bi-directional control method for the inductorless half-bridge topology [9, 36, 39].

F. Comparison and examples

Table I shows some examples of investigated topologies with claims of efficiency and output power level and Table II shows an overview comparison of the most popular PT-based converter topologies from prior art study.

III. NEW CHALLANGES

PTs use electromechanical coupling between the primary and secondary sides compared to conventional transformers that use electromagnetic coupling. This introduces PTs as applicable candidates for applications which have a high sensitivity to electromagnetic interference, e.g. magnetic resonance imaging (MRI) scanners. Therefore, PTs with non-magnetic drivers may be able to work in high electromagnetic fields, e.g. 7 Tesla.

This section proposes challenges for PT-based power drivers and possible solutions based on the state-of-the-art technology for addressing these challenges.

A. Challenges for PT

Challenges for the design of PTs are:

- To increase power density: results in higher power transmission into the output of converter. It is limited by design and production factors.
- To raise power transmission capability: leads to have simpler converters and control techniques by utilizing as few PT as possible.
- To combine PTs, creating new techniques for increased power through output: e.g. a method of connecting PT-based converters for the output voltage summation is proposed in [24]. Suggestion for combination methods depends on the application and it is important to avoid complexity in circuit design.

TABLE I. Efficiency and power level examples

Topology	***Push Pull***	***Class E***		***Half-bridge Inductorless***		
Efficiency(%)	70	82.4	70.5	58.5	90	90
Power[W]	2	3.6	3.6	3.6	32	6.5
Reference	[15]	[19]	[19]	[37]	[25]	[28]

TABLE II. Comparison of most popular PT-based SMPS topologies

Topology	*Application*	*Control*	*Efficiency*	*Power level*	*EMI*
Push-Pull	Step-up Higher ratio than half-bridge [7]	Simple Output current control [16]	86% [16]	Low	Yes (Inductor)
Class E	Step-down Power application [7]	PLL	82.4% [19]	High [17]	Yes (Inductor)
Class D/ Half-bridge	Step-down Power application [7]	Phase shift Forward conduction mode [28] Burst mode [37]	90% [28]	Very high [9, 19]	No (Inductorless)

B. Challenges in power stages

Energy recovery through bi-directional current flow is critical for achieving high driver efficiency. As energy is directed back from the output side, the properties of the PT change dramatically, e.g. soft switching ability. Therefore achievable ZVS is required for both forward and reverse power flow directions. This imposes strict requirements on the driver design. The driver should allow for suitable control of the PT, and techniques for obtaining high efficiency and compact converter which these call for new solutions. If the load is capacitive piezoelectric actuator, bi-directional current flow requires advanced control schemes to allow precise control of the capacitive load. According to the prior art, half-bridge topology and the self-oscillating control loop based on the phase shift control method can be selected for resolving this challenge. Furthermore, in case of using several PTs for increasing the demanded output power, more complex control loops is required to combine converters together.

IV. CONCLUSION

In this paper, the principle of state-of-the-art PT-based SMPS has been studied with the aim of appraising important considerations in the design of converters. In the prior art section, major factors in PT design have been reviewed, as well as the soft switching capability of PTs which allows obtaining ZVS in the converter and a decrease of switching losses. The main focus of this paper has been researching power stage topologies and control methods used in prior art and their applications. Research in this paper shows inevitable implementation of one or more control loops for better performance of PTs and converters, and the correlation between efficiency, losses, temperature and frequency.

Furthermore, new challenges for future research are introduced both in PT design and in power stages, with a guide to topology and control method selection.

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Appendix C

Power enhancement of piezoelectric transformers for power supplies

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Accepted for

Conference on Power, Electronics, Machines and Drives (PEMD 2016)

Power enhancement of piezoelectric transformers for power supplies

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Keywords: Piezoelectric transformer; piezo actuator drive; power enhancement.

Abstract

This paper studies power enhancement of piezoelectric transformers to be used in inductorless, half-bridge, piezoelecteric-based switch mode power supplies for driving a piezo actuator motor system in a high strength magnetic environment for magnetic resonance imaging and computed tomography applications. A new multi element-piezo transformer solution is proposed along with a dual mode piezo transformer, providing power scaling and potentially improving the internal heat-up of a high power piezo transformer system.

1 Introduction

The Piezo actuator drive (PAD) is a drive technology transforming the linear motion of high performance piezoelectric multilayer actuators into a powerful and precisely controllable rotation. PAD aims to enable reliable motor performance in strong magnetic fields for magnetic resonance imaging (MRI) and computed tomography (CT scan) treatment tables. There are some limitations in the current treatment tables, e.g. motors cannot operate in the presence of strong magnetic field inside the MRI room. Furthermore, imaging and motor operation cannot take place simultaneously. PAD characteristics, i.e. nonmagnetic high speed independent torque, integrated force and position feedback allow for better performance and higher flexibility in the construction of treatment tables. However, there are technological limitations in operation of this motors and drive systems related to magnetic interference. The creation of a motor based on the PAD principle, exhibiting nonmagnetic behaviour which requires the development of innovative driver solutions for the piezoelectric actuators. Moreover, designing a nonmagnetic driver for providing power to the PAD motor is quite challenging since the driver also should be nonmagnetic. Piezoelectric transformers (PTs) are suitable candidates for addressing this challenge to provide solutions, which are far beyond any existing technology.

Employment of PT has become popular since it can replace magnetic and reactive components in both resonant and traditional magnetic transformer-based converters due to smaller size, lighter weight, lower cost, lower electromagnetic interference (EMI), higher power density, and higher efficiency [1]. The operating principle of the PT is based on electromechanical energy conversion. PTs use electromechanical coupling between the primary and secondary sides compared to conventional transformers which use electromagnetic coupling. This introduces PTs as applicable candidates for applications that have a high sensitivity to electromagnetic interference [2]. Therefore, PTs with nonmagnetic drivers may be able to work in high electromagnetic fields, e.g. 7 Tesla. Transmitted energy ratio in PTs cannot exceed 95% due to piezoelectric material losses [3], but a proper design is needed to benefit from maximal obtainable power density.

This paper is organized as follows. Section 2 presents challenges and short comings in power capability of PTs for driving a piezo actuator. The solutions for enhancing PT's power throughput are introduced, designed and investigated. Furthermore, explanation about construction method and mounting is provided. Results of different designs are compared and explained in the Section 3. Finally, the conclusion is provided in section 4.

2 Challenges

This Section deals with detailed explanation of requirements for PTs and design methodology used for increasing the power throughput of transformers.

2.1 PAD

The PAD shown in Fig.1 consists of four single piezo actuators (PAs) with capacitive behavior. Structure of one PA is shown in Fig. 2. Theoretically, power level of up to 100 W is needed to drive a PA placed inside the PAD motor. The maximum output power density of piezo transformers are limited to around 52 W/cm3 [4] which depends on the type of the piezo ceramic. The most two important keys in design of transformers have been thermal management and power scalability. Providing the required power through a PT for one single element is quite challenging due to limited technology of PTs. The PT generates heat during operation and this causes considerable changes in its operating point and consequently voltage gain. The main target for reduction of self-heating has been to reduce the interlayer thickness and

keep the power density to a certain level. However, the PT should be capable of transferring large power to the PA to drive the PAD motor. Furthermore, having nonmagnetic driver implies that the PT should be capable of handling massive power peaks and do this without the help of coils to support soft switching for the converter methodology. This arises need for new solutions, which is of the interest of this research.

Figure 1: PAD motor.

Figure 2: Piezo actuator as a load of the driver.

2.2 PT's power enhancement

This paper studies power enhancement of PTs to be used in inductorless, half-bridge, PT-based SMPS [2]. The transformer type is selected to be interleaved interdigitated electrode (IDE) multilayer PT, regarding easy manufacturing as well as high efficiency advantages by utilizing longitudinal mode vibration [5]. In this work two solutions are suggested and designed to raise the power capability of the PT. New ideas are designed, fabricated and tested for the purpose of this work. The first solution is multi-piezo element and the second one is scaled-size PT. Both solutions are for obtaining higher power transformation by keeping the same power density to avoid thermal increase. Fig. 3 shows design simulation of a PT element which is used as a root element of further designs. The root element is constructed as a true piezo transformer in regards to temperature, zero voltage switching and voltage gain.

The first design uses a configuration with extended width to excite the first thickness mode operation as well as a standing wave across the width of the PT structure. Although this may prove difficulty to tune, it has a wide potential for a powerful transformer configuration with low internal heat generation due to the large power generating zone. Fig. 4 shows simulation results of scaled-size PT at the resonance frequency. The second design is a combination of multi root elements in one block. Every two adjacent elements are polarized in the opposite directions; hence three individual PTs are presented in the structure. In this design there are nineteen electrodes accessible for polarization. Therefore, polarization is a difficult task from the research point of view, but in mass production this will not be an issue. The major benefit is that this design potentially solves the power scaling issue of PTs, since a whole PT block can resonate at the resonance of a root PT design. In other hand, its entirety contributes linearly to the output power. This property becomes important in this application since the power levels are needed to be extended beyond the capabilities of the theoretical limit of a single PT element in terms of stress and material properties. Fig. 5 shows the fabricated transformers.

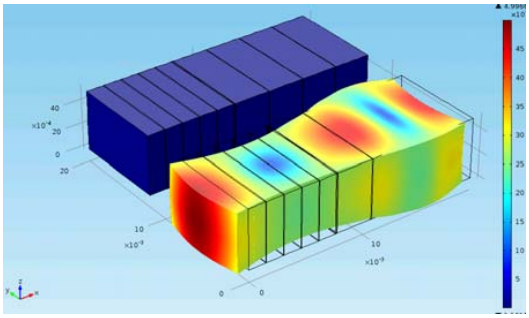


Figure 3: The root element of piezoelectric transformer. Simulation is done in COMSOL Multiphysics and shows operation of the root element in its first resonance mode. The colour blue illustrates the point of maximum stress but minimum deformation.

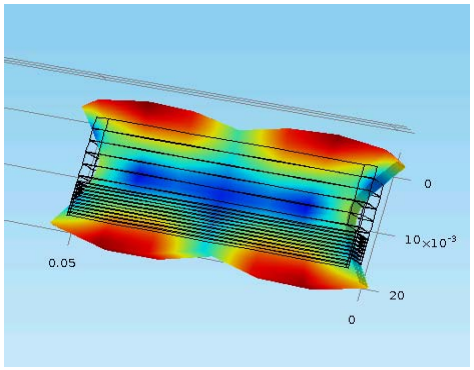


Figure 4: The scaled-size PT is a large transformer that utilizes a multimode approach for obtaining the required stresses for energy transfer. Please note the extended blue area where the PT can be mounted.

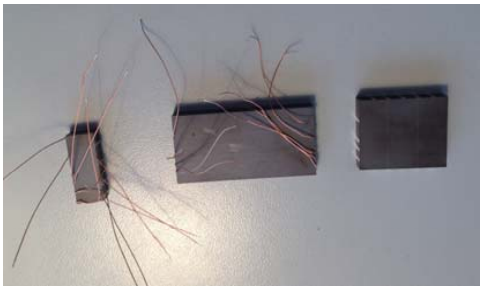


Figure 5: All of key transformers side by side; from left to right – The root element; the scaled-size PT; the multi element PT with three active root elements mechanically coupled together.

2.3 PT construction method

During the construction of the PT elements either hard or soft-doped piezo ceramic materials could be used. For a resonating transformer usually a hard-doped ceramic is used, due to the stiffness and very high Q factor, which is often associated with these types of ceramics. The material selected was NCE46 provided by Noliac A/S. The material is well understood and provides the necessary flexibility in prototype production. However the material demands that all of the internal electrodes to be comprised of Platinum/Palladium, instead of Silver/Palladium as seen in other builds due to the high sintering temperatures needed for this material.

To construct the piezo structures proposed in this paper, the selected build-up method is the newly developed IDE stacking process, which allows the producer of piezo components to make virtually any thickness mode design since each PT is constructed from a series of piezo layers that is stacked with very accurate positioning. With this new technology, a PT operating in thickness modes becomes possible which leads to multiple geometrical shapes that can be realized in the prototype development stage. For our selection, we have chosen to build an IDE transformer that is square allowing for maximal usage of the whole piezo wafer, therefore increasing our yield per production.

Furthermore, this technology allows for many different designs in one singular build-up to easier spread the risk, and since an isolation layer is needed, analogies to that of a regular magnetic transformer, an IDE based transformer only needs one section instead of the radial mode solution that had to have two sections of isolation – due to the symmetrical build-up principles in place for a stable radial mode transformer.

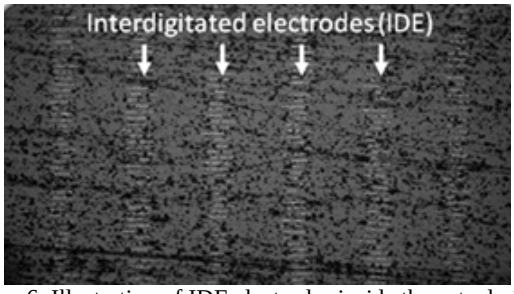


Figure 6: Illustration of IDE electrodes inside the actual piezo transformer

One downside to this build process is that the minimum production qualified electrode thickness is a 70 [µm]. This means that we are going to have some inactive material that does not generate electrical energy but reduces the energy transferring mechanisms, which cannot be avoided at this point.

2.4 Mounting the transformers

Since the two mentioned transformers will operate at two different modes (the first and the second mode, respectively) this also leads to two different mounting strategies as seen in Figure 7. The main aim for the authors mounting strategy is to minimize the damping from fixing the transformer in place. However, from heat-buildup analysis, it has been found that mounting the transformer at the nodal point(s) will not only provide an undamped fixing of the PT, but also provide a method of shunting most of the heat away from the PT. This is derived from the analytical work on zero voltage switching (ZVS), that discovered the area of maximum internal stresses inside the piezo structure is also responsible for the majority of the heat generated by the PT, hence it could be recommend that the mounting bracket of a PT should also be capable of heat transference in high stress high frequency operation.

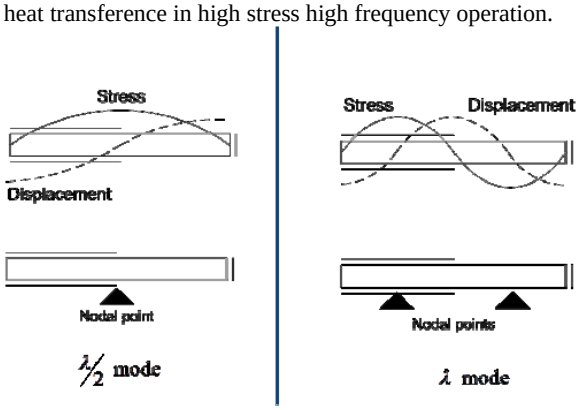


Figure 7: Mounting piezo transformers is preferably done at the point of maximum stress, which is the point of minimum displacement.

3 Results

From simulation results it became obvious, that matching the desired operational frequency and geometry lead to the process of adding or subtracting material of the PT in order to tune to the correct frequency of the transformer. Furthermore, it was experienced that the polarization of the PT become more and more difficult along with the length increase of the PT, since the polarization happens roughly around 10 times the normal operation voltage and the polarization happens more or less rapid at a certain voltage level allowing for a shock to travel through the entirety of the structure creating chipping or breakage. In many cases the achieved power levels were somewhat comparable to the simulated results, but in high strain PT structures it is was clear that temperature increase hindered further power throughput. It was found that this might be linked to the ZVS capabilities inherent to this design and some investigation on ZVS leading to increase in thermal losses concluded that this presumable is the case. The ZVS result was interesting since is also partly states that stresses beyond certain levels inside the PT forces the PT to become much more thermally active. As seen in the Figure 8.

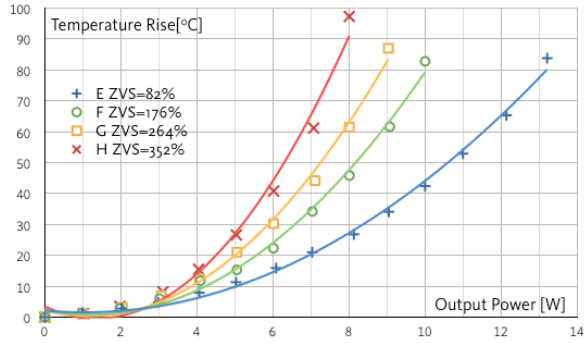
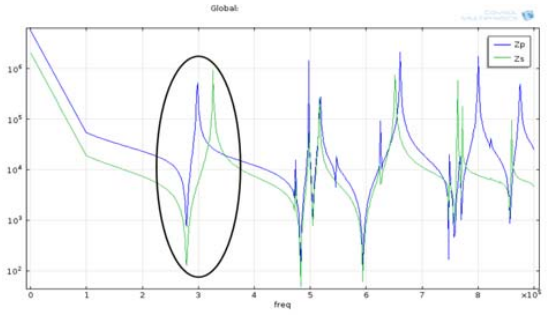


Figure 8: Heat generation at different ZVS levels and throughput.

Concerning the resonance of the system it was found that a piezo design with a low ZVS also provided another interesting feature since a ZVS close to 100% would in some sense be better for a bi-directional transformers since a ZVS of 150% forward conduction mode would be a unmatched system at bi-directional operations see Figure 9.



Figurer 9: Impedance plot of the given test system

4 Conclusion

In this research two possible PT solutions are proposed and tested. Furthermore, this paper dealt with power enhancement of PT in order to be able to transfer enough energy for driving a piezo actuators placed inside the PAD motor. Increasing power transmission capability of PT has led to an array of interesting observation that launched analysis on ZVS capability and stress buildup inside the PT unit, as a result from the excess heat generated by the prototype samples. Furthermore, a novel suggestion of using a multiple of PT operating in thickness mode coupled together in one single unity was proposed to tackle the power scaling issue that operating the PAD motor poses.

Acknowledgements

The authors would like to thank Noliac A/S for supplying prototype of piezoelectric transformers as well as "The Danish National Advanced Technology Foundation" for their financial support.

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Appendix D

Digitized self-oscillating loop for piezoelectric transformers for power supplies

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Accepted for

The Applied Power Electronics Conference and Exposition (APEC2016)

Digitized self-oscillating loop for piezoelectric transformer-based power converters

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***Abstract*—A new method is implemented in designing of self-oscillating loop for driving piezoelectric transformers. The implemented method is based on combining both analog and digital control systems. Digitized delay, or digitized phase shift through the self-oscillating loop results in a very precise frequency control and ensures an optimum operation of the piezoelectric transformer in terms of voltage gain and efficiency. In this work, additional time delay is implemented digitally for the first time through 16 bit digital-to-analog converter to the self-oscillating loop. Delay control setpoints updates at a rate of 417 kHz. This allows the control loop to dynamically follow frequency changes of the transformer in each resonant cycle. The operation principle behind self-oscillating is discussed in this paper. Moreover, experimental results are reported.**

***Index Terms*—Optimum delay line; self-oscillating loop; phase shift; switch mode power supply; zero-voltage switching; piezoelectric transformer.**

NOMENCLATURE

BPF	Band pass filter.
C	Resonant capacitance of the piezoelectric transformer.
C_A	Measurement capacitance.
C_{d1}	Input electrode capacitance of the piezoelectric transformer.
C_{d2}	Output electrode capacitance of the piezoelectric transformer.
CEZC	Current estimate zero crossing.
D	Duty cycle.
DAC	Digital-to-analog converter.
DDL	Digitized delay line.
DDL_{out}	Output of the DDL.
DT	Dead time.
$EDDL_{in}$	Edge detected of the input of the DDL.
FF	Flip-flop.
FPGA	Field-programmable gate array.
$i_{res}(t)$	Piezoelectric transformer's resonant current.
L	Internal inductance of the piezoelectric transformer.
LPF	Low pass filter.
MOSFET	Metal-oxide-semiconductor field-effect transistor.
PT	Piezoelectric transformer.
R	Dielectric losses inside the transformer.
R_A, R_B	Sensing resistors.
R_L	Load resistor.
$R_{matched}$	Matched load for the piezoelectric transformer.
$v_F(t)$	Switching voltage in the primary side of the PT.
ZVS	Zero voltage switching.
ω	Angular frequency.
ϕ_I	Phase shift of the resonant current.

I. INTRODUCTION

Piezoelectric transformers' (PT) voltage gain, resonance frequency and efficiency change with variation of their load and temperature [1]–[4]. Therefore, in order to operate a PT in its optimum point, located slightly above the resonant frequency, it is necessary to follow changes in the resonance frequency [1]. It is required that the self-oscillating loop be able to adjust its phase shift to follow the PT's resonant frequency. Therefore, implemented adjustable phase shift compensates for the rest of the phase shift in the loop for frequency variations. For instance, when the energy transfered by the converter needs to be controlled to maintain DC output voltage at different voltage levels, the PT's load changes. Any changes in the PT's load causes a change in its operating point [4]. In order to keep the PT operating at its most efficient point, its operating frequency should be changed. This is per-

formed by changing the converter's switching frequency. The switching frequency is controlled through a self-oscillating loop. Therefore, by changing the predesigned phase shift, the switching frequency follows variations in the PT's resonant current.

Phase shift compensation with high resolution becomes necessary especially when the load of the converter is variable. These variations directly translates to the PT's load variations. If the total phase shift of the loop is not properly adjusted to an integer factor of 360°, it causes a damping of the resonant current and, the closed-loop operation cannot be achieved, so the converter will not start working. Therefore, very fine resolution for the phase shift adjustment is required.

In previous research, an adjustable time delay block that controls the total phase of the loop has been implemented through an analog circuit. In the closed-loop operation, 360° phase difference in the desired frequency cannot be ensured for the load or temperature variations of the PT [5], [6]. To solve this problem, a digitalized phase shift compensation is applied in this paper. Changes in the PT's resonant frequency are compensated for the closed-loop by detecting and adding required phase shift in order to obtain a full loop phase shift of 360°. Compensation is performed by adding a finely-controlled time delay to the feedback chain. Resolution of the applied time delay is 1 ns. This ensures that the added time delay is finely controllable in order to precisely adapt the frequency of the self-oscillating loop and match changes in the PT's operating point. Furthermore, the delay can work in the range between 0° to 180°. This then, further ensures soft switching operation of the PT and efficiency increase.

This paper is organized as follows. Section II presents thorough explanation of the self-oscillating loop. Subsections II-A and II-B explain the principle behind self-oscillation in the prior art. Section II-C shows experimental results. Section III-A gives more explanation about the proposed method and subsection III-B shows experimental results for the proposed method.

II. Self-oscillating loop for PT-based converters

A. Principle and design considerations

Essentially, two requirements need to be satisfied in order to produce sustained oscillation in a closed-loop. One is that phase angle of the whole loop should be an integer multiple of 360°; the other requirement is that the loop gain should be greater than unity to start up the oscillation. The former condition is fulfilled by adjusting phase shift through the loop. The latter condition is fulfilled by the use of a comparator since the comparator's gain can be considered infinite and therefore its input becomes saturated to the rail voltages. This results in generating square waves in the output of the comparator.

Fig. 1 shows the circuit for the self-oscillating loop together with the PT-based power stage with matched load, $R_{matched}$. Fig. 2 shows the block diagram for the self-oscillating loop [7]. A small perturbation in the loop starts the self-induced oscillation. This results in self-excitation of the resonant current inside the PT during the start-up. Self-excited square waves with a frequency lower than or close to the resonant frequency of the PT will excite resonant modes inside the transformer. This is achieved by the fundamental frequency of the square waves. Since the PT is operating as a high quality factor (Q) band pass filter (BPF), it filters higher order harmonics out and transfers the fundamental component to its output. The electrical quality factor of the PT is derived as:

$$Q = \frac{1}{\omega C_{d2} R_L} \tag{1}$$

where $\omega = 1/\sqrt{LC}$ is the series-resonance angular frequency of the PT [8]. Therefore, the resonant current is considered as a sinusoidal waveform and is described as

$$i_{res}(t) = I_{pk}(t)\, sin(\omega t - \phi_I) \tag{2}$$

where $\phi_I \in [0, \pi]$ is the current phase angle.

The amplitude of the fundamental resonant current grows with time until it reaches to a certain level that the self-oscillating loop becomes locked at the resonant frequency. Since the amplitude of the sinusoidal waveform at the output of low pass filter (LPF) shown in Fig. 2, becomes greater than the amplitude of the self-induced oscillation waveform, the oscillator operates as a comparator. This allows the comparator's behavior to change from that of an oscillator to that of a true comparator. Therefore, it compares the resonant current with a DC level in order to mark the zero crossing of the current. The loop is designed for the case in which the PT is connected to the resistive matched load [7].

$$R_{matched} = \frac{1}{\omega C_{d2}} \tag{3}$$

The reasoning behind this design choice is that a matched load is considered to be the worst case scenario for a PT, in terms of achieving soft switching [9]. Zero-voltage switching (ZVS) is a form of soft switching considered in this work. At the matched load, the energy

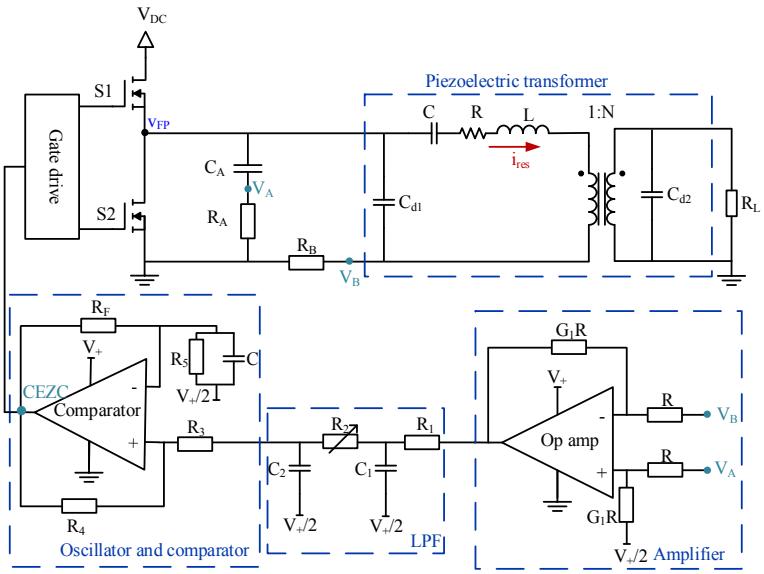

Fig. 1: Circuit design of self-oscillating loop in the PT-based SMPS.

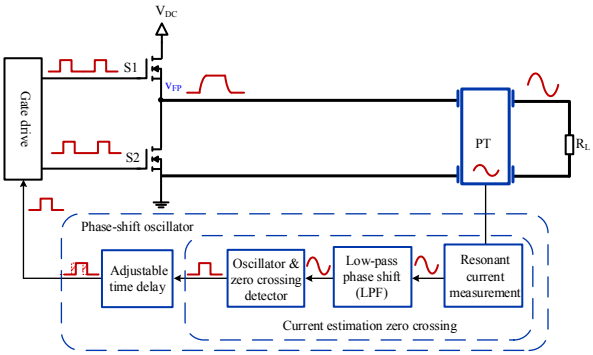

Fig. 2: Block diagram of the self-oscillating loop from the previous research.

transfer through the PT is maximum and therefore its efficiency is maximized as well. This results in a point of minima on the ZVS factor axis [4], [10]. The role of the ZVS factor is to provide the worst case scenario for analyzing PTs in terms of soft switching capability, which means that if the ZVS is achieved for the matched load, it will be obtained for other loads as well [9]. The worst case explanation of the approximated ZVS factor is expressed based on empiric analysis of the ZVS in the following equation [11]:

$$V_p' = (0.304\ \frac{1}{n^2}\frac{C_{d2}}{C_{d1}} + 0.538) \cdot (0.585\eta + 0.414) \quad (4)$$

where η is the efficiency of the transformer. V_p' is the ZVS factor and should be above 1 in order to obtain soft switching. Therefore, the ZVS region is a narrow frequency range above the resonance frequency, where the PT behaves as an inductor and $V_p' > 1$. Furthermore, the ZVS bandwidth of the PT is a ratio of L/C for a constant resonance frequency [9]. Equation (4) is based on a primary analysis of ZVS in order to justify the necessity to design a driver and the self-oscillating loop.

B. Current estimation zero crossing (CEZC)

The resonance current in the PT is reconstructed within two time intervals. Voltage V_B across R_B shown in Fig. 1 measures this resonance current while the switches are on. Voltage V_A across R_A measures the resonant current during dead time (DT), while both switches are off. The resonance current in this period is supplied by the PT's input capacitor C_{d1}. Therefore, the current passing through C_{d1} follows the resonant current and can be measured by differentiating the voltage across C_{d1}. This is performed by using C_A and R_A as a differentiator. By proper subtraction of these two voltage waveforms through the op-amp, an approximate sinusoidal waveform representing the resonant current will be reconstructed in the output [7], [12], [13].

The estimated current has a 180° phase shift compared to the resonance current which results in the same zero crossing points. Thereafter, the estimated resonance current is transmitted to a second order LPF which

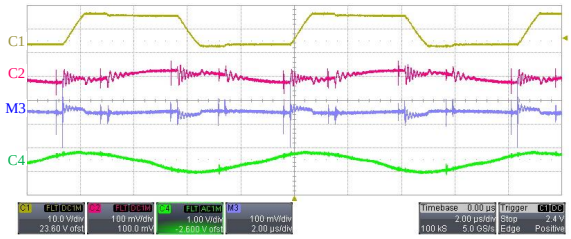

Fig. 3: Reconstruction of the resonant current. C1: switching voltage v_F, C2: the voltage V_B, M3: the voltage V_B, C4: voltage output of the op-amp Gain.(V_A - V_B)

Fig. 4: CEZC board

provides an additional phase shift through the feedback loop. The filtered signal is transmitted to the comparator and generates a square wave indicating the zero crossing of the input signal. The square wave signal is fed into the adjustable time delay in order to compensate for the rest of the phase shift to have a total phase shift of 360° in the entire loop from the input of the gate driver to the output of feedback loop. In case the switching frequency needs to be decreased, the total phase shift should be increased. Additional phase shift in the loop is added through a digitally-controlled time delay. Since time delay is a positive value, the controlled delay adds an adequate phase shift in order to synchronize the frequency in the next cycle.

C. Experimental results

A radial mode PT with Mason's equivalent circuit, shown in Fig. 1, is used, driven by square wave signals with a switching frequency of 118.3 kHz, while driving a resistive load of 300 Ω. Moreover, reconstructed resonant current from voltages V_A and V_B is shown in Fig. 3. The designed board is shown in Fig. 4. Fig. 5 shows experimental waveforms for the self-oscillating loop. Phase shifts and corresponding time delays between stages are measured and shown in table I. Furthermore, the equivalent parameter values of the PT are measured and shown in Table II.

TABLE I: Phase shifts during one switching cycle in the self-oscillating loop; switching frequency is 118.3 kHz with the time period of 8.45µs.

Delay	Time [µs]	Phase [°]	Duty cycle %
HS→HSGD	1.59	67.8	18.85
HSGD→I_{est}	0.27	11.5	3.19
I_{est}→LPF	6.09	259.4	72.04
LPF→CEZC	0.5	21.3	5.92
Total	8.45	360	100

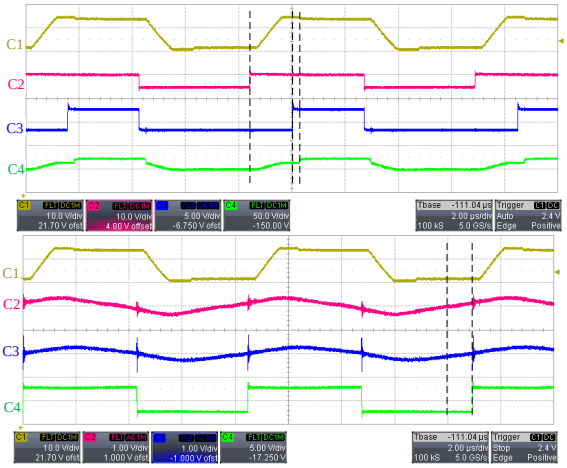

Fig. 5: The self-oscillating loop in the previous research; wave forms from top to bottom show outstanding phase shift during one switching cycle. On top: C1: the switching voltage (v_F); C2: CEZC; C3: input signal to the high-side gate drive; C4: high-side gate drive output to the ground. On bottom: C1: switching voltage (v_F); C2: estimated resonant current in the output of op-amp; C3: estimated resonant current in the out put of LPF; C4: CEZC.

TABLE II: PT equivalent parameters

Parameter	Value	Parameter	Value
C_{d1}	3.8 nF	C_{d2}	626 pF
C	565 nF	R	5.6 Ω
L	3.5 mH	N	3.5

III. Digitized Delay Line (DDL)

A. Design considerations

Initial investigation of the time step resolution shows need for a finely adjust of the total delay in the loop. The result of this investigation showed that there was a change in the amplitude of the PT's output voltage for every 10 Hz change in the switching frequency. For example, if the operating frequency of 100 kHz increases by 10 Hz, the output voltage shows a considerable change in the amplitude. Therefore, a precision of minimum 10 Hz in the frequency is required for a

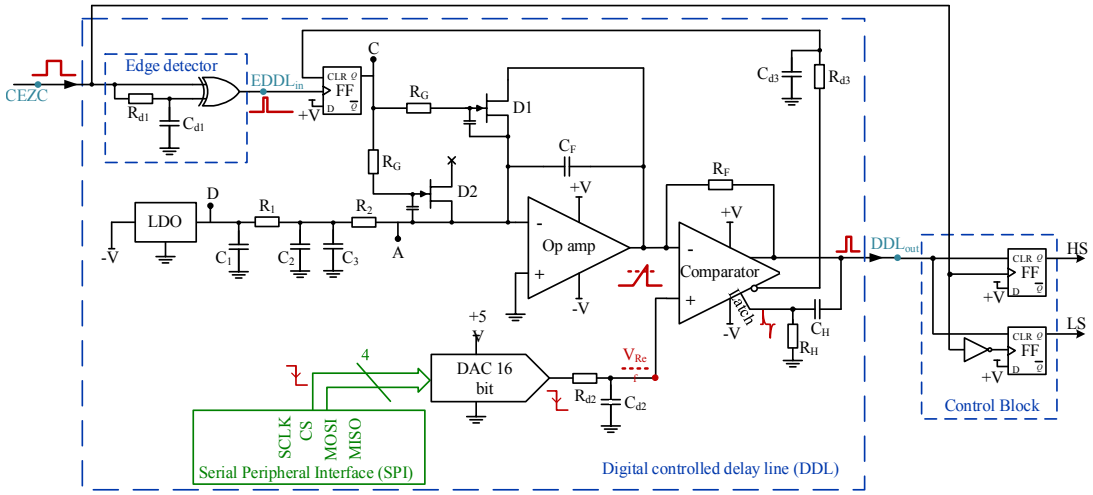

Fig. 6: The electrical circuit of the DDL block, with resolution of 1 ns.

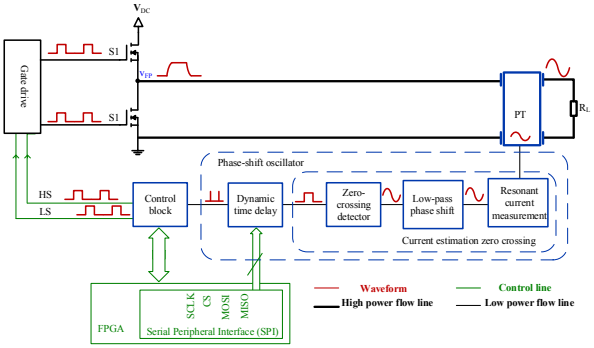

Fig. 7: Block digram of self-oscillating loop with dynamic time delay.

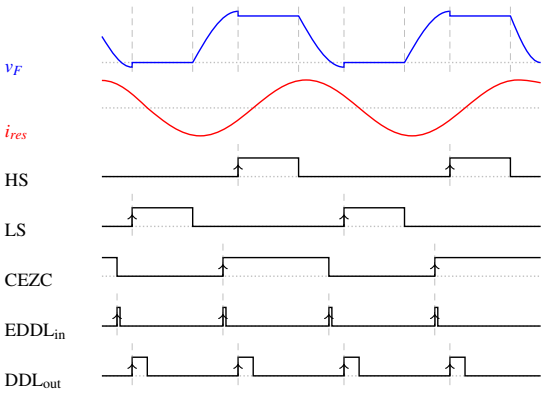

Fig. 8: Signal waveforms with negligible propagation delays in digital gates and the gate driver.

dynamic time delay which is equivalent to 1ns resolution. Fig. 6 shows a simplified version of the circuit used as a control block. Fig. 7 shows the block diagram of the self-oscillating closed-loop together with the contribution of the digital-to-analog converter (DAC) and field-programmable gate array (FPGA). These are used to implement a high-resolution time delay inside the DDL block.

Fig. 8 shows a detailed drawing of the main signal waveforms in the circuit. $v_F(t)$ is the transformer's primary-side voltage while exhibiting soft switching. $i_{res}(t)$ shows the resonance current of the PT. This current is dependent on the characteristic parameters of the PT and it changes its polarity when either the switches are on or their body diodes conduct. Therefore, depending on the operating frequency and temperature of the PT, there is a phase shift between the resonance frequency and the switching voltage, that is defined as ϕ_I in (2). Consequently, it is important that the circuit is capable of compensating for this phase shift. The estimated resonance current shown in Fig. 7 passes through a 180°phase shifter, then a LPF and a comparator. This is illustrated in Fig. 8. The output of the CEZC block which has the same frequency as the resonance is then tied to the DDL block. In DDL block, the input signal is first transformed into edge-detecting one-shot pulses ($EDDL_{in}$) which are then used as a clock source for the flip-flop (FF). The signal from this FF is then used to reset the hardware integrator present in the circuit. Namely, when the input signal edge-triggers the FF, the feedback capacitor in the op-amp feedback starts

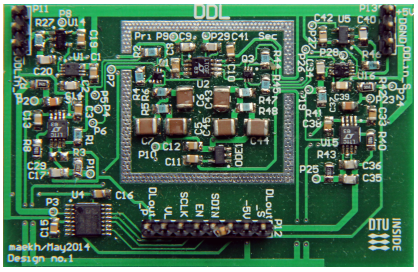

Fig. 9: DDL board

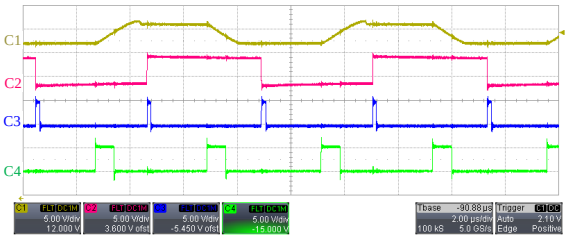

Fig. 10: Measurement: Signal waveforms where dynamic delay is applied; C1: switching waveform (v_F); C2: CEZC as input of the DDL block; C3: one-shot pulse $EDDL_{in}$; C4: output of the DDL block (DDL_{out}).

charging, thereby creating a fixed voltage slope. This is then compared to the variable reference voltage provided by the DAC. Thereafter, the complementary output of the comparator resets the FF which consequently turns the MOSFET, D1, on and discharges the feedback capacitor, thereby resetting the integrator. Since the input pulse triggers the start of the integration, the variable reference provided to the comparator by the DAC coupled with the voltage slope work together to create a time-delayed version of the input pulse which is proportional to the DAC output value. The output of the comparator is then latched for a short time by its own output through a high-passed signal to its latch pin, resulting in one-shot pulses at the output of the DDL.

The output of the DDL is capable of prolonging the switching period by changing the duty cycle of the switches (D). The high-side and low-side switches are turned on by rising edges of CEZC and $\overline{\text{CEZC}}$ signal, respectively, which are used as clock inputs to the control block FFs. The output of the DDL block is then used to reset the flip-flops, thereby turning the switches off. Dead time (DT) is fixed for a specific design regarding a certain PT and switching frequency. Since this DT is fixed, by adjusting the time-delay for turning the switches off, the frequency of self-oscillation changes. DDL block delays its input (CEZC) to compensate the rest of phase shift through loop to reach 360°. The propagation delay in the control block is assumed negligible in the waveforms shown in Fig. 8.

B. Experimental results

A prototype has been built and tested. Fig. 9 shows designed modular board for DDL block. A radial mode PT with Mason's equivalent circuit is used, driven by square wave signals with a switching frequency of 118.3 kHz and a resistive load of 300 Ω. Furthermore, the equivalent parameter values of the PT are measured and shown in table II. Input signal waveform of DDL circuit i.e. CEZC and one-shot input pulse together with the output of DDL are shown in Fig. 10. Table III shows measured phase shifts and corresponding time delays between stages.

TABLE III: One cycle phase shift measured in the self-oscillating loop

Delay	**Time [µs]**	**Phase [°]**	**Duty cycle %**
HS→HSGD	0.28	11.94	3.3
HSGD→I_{est}	6.6	281.52	78.2
I_{est}→ LPF	1.56	66.5	18.5
Total	8.44	360	100
D:$EDDL_{in}$→DDL_{out}	2.5	106.6	29.6

IV. Conclusion

General operation of a self-oscillating loop for piezoelectric transformer-based power converters is explained. The designed circuit for operating the transformer together with experimental results are provided. The circuit is based on a new idea for compensating and controlling the phase shift for the self-oscillating in order to achieve and maintain soft switching. This is combined with a resonance current estimation that is able to start and maintain the circuit oscillation. The operation of and cooperation between the analog resonance current estimator and digital phase shift adjustment are presented in detail, together with some insight into the performance of the designed circuit. The concept is proven through the experimental results. 1 ns time step resolution is sufficient for adjusting the phase shift of the loop. The designed circuit is able to follow changes in the resonance frequency of the PT in every cycle.

Acknowledgment

The authors would like to thank Noliac A/S for supplying the prototype of a piezoelectric transformer as well as "The Danish National Advanced Technology Foundation" for their financial support.

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Appendix E

Bi-directional high-side current sense circuit for switch mode power supplies

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Presented at

IEEE International Conference on Electronics Circuits and Systems (ICECS 2014)

Bi-directional high-side current sense circuit for switch mode power supplies

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***Abstract*— In order to control a power supply using piezoelectric transformer, AC current in the transformer needs to be measured. Due to the control strategy it is necessary to measure amplitude, phase angle and zero crossing of this current. In some applications there is common ground between primary and secondary sides of the transformer which is internally implemented inside the transformer. Therefore, current must be measured from the high voltage line in the presence of high input switching voltage. This paper proposes a resistive current sensing circuit based on discrete components useful for input voltages on the order of 200 V. The bandwidth is at least 200 kHz to allow fundamental frequency detection of piezoelectric transformers in use.**

Keywords—High side current sense, resisitive current sense, high common mode voltage, piezoelectric transformer

I. INTRODUCTION

Current sensing in power converters is critical for purposes involving closed loop control and power measurement [1]. Different current sensing techniques are normally used for different applications e.g. resistive sensing (discrete resistors, copper resistors) or magnetic sensing. The most commonly used technique for measuring electrical current is resistive current sensing [2]. However, in a system with large input voltages the input common mode voltage is larger than what can be handled by standard methods for measuring small differential voltages across a sense resistor. This is mainly a major challenge for measuring the differential voltage [2]. Furthermore, having adequate bandwidth in the presence of high common mode voltage brings more challenges in some applications.

In this paper a new bi-directional current sensor is designed by employing resistive current sensing. The application is to be used in the high side of the half-bridge topology in a piezoelectric transformer (PT)-based switch mode power supply (SMPS). This current sensor allows differential signal measurement in the presence of a high common mode voltage (up to 200 V) across the sense resistor with an effective bandwidth of 200 kHz. Measuring the signal current through the resistive sensor with a high common mode voltage is a challenge as standard differential amplifiers cannot handle input common mode voltages of this magnitude. Furthermore, the influence of switching noise in this particular place of interest which is directly connected to the switching node complicates the measurement. Consequently, commercial available high side sensors could not fulfill requirements for the converter in use with respect to maximum common mode voltage and required frequency bandwidth.

Since amplitude and phase of the resonant current inside the PT varies with changes in frequency, load and temperature, it is necessary to measure the resonant current. Moreover, switching frequency depends on the operating frequency of the PT which is different from one PT to another. Therefore, it is necessary to have a broad frequency range for detecting resonant current. The measured current can be utilized for control of the PT operating point. In general there is no access to the series resonant current inside the piezoelectric transformer. Thereby, some techniques should be employed to measure this current.

In this application measurement of resonant current during the on time of switches through the high voltage line of the class-D amplifier is of particular interest. The current sensing circuit is considered as a current to voltage converter, basically comprising a sense resistor and a level shifting circuit to shift the common mode voltage level for the sense resistor to a low voltage level which can be handled by standard op amp circuits using small values of supply voltage. The output voltage from the level shifter is the same as the differential voltage across the sense resistor and can directly be used for further signal processing using analog or digital techniques.

In section II of this paper the basic current sensing circuit is described and analyzed. In section III the functionality of the circuit is validated by simulation results. Finally, section IV provides the conclusion.

II. SENSING CURRENT CIRCUIT

A. Theory and design

In this work focus has been on providing a bi-directional current sensing solution for a PT-based SMPS. A sense resistor is put in the high side rail between the switching node and the primary side of the PT. Fig. 1 shows block diagram of the converter in use. For the power stage, PT-based power converter with matched load has been used. The current sensor

is put on the high voltage line in the primary side of the transformer for sensing resonant current in the presence of high common mode voltage. The output voltage represents the current flowing through the sense resistor (R_s) by transferring current to the voltage (V_S) with an amplification factor of K.

The current through the sense resistor will be the same as resonant current when switching voltage is clamped either to zero or positive rail by turning on the MOSFETs or even when their body diodes conduct. Voltage across the sense resistor is directly proportional to resonant current in these perifods.

Fig. 2 shows the circuit designed to provide the level shifting from the input voltage of the sense resistor to a voltage which is referenced to the negative supply voltage $-V_{EE}$. The circuit utilizes bipolar transistors with a high maximum value of V_{CE} in order to accommodate a large input voltage swing. The transistors Q_1 to Q_6 form a current mirror which is degenerated by the voltage drop across the sense resistor. Hence, the current in the input side of the mirror (Q_1 and Q_4) is different from the current in the output side (Q_2 and Q_5) and the difference depends on the voltage drop V_S. Transistors Q_3 and Q_6 are inserted to minimize the influence of the base currents required for Q_1, Q_2 and Q_4, Q_5. Transistor Q_7 together with the resistor R and Q_9 forms a constant current source. Neglecting the base current of Q_3 and Q_6 the current from this current source will flow in Q_1 as indicated in Fig. 3. A simplified analysis of the current mirror (neglecting base currents) yields

$$I_1 = I_s e^{-V_{BE}/V_T} \tag{1}$$

Where, I_s is the transistor saturation current and V_T is thermal voltage (approximately 25 mV at room temperature). By substituting I_1 in the similar equation for Q_2, I_2 can be expressed as:

$$I_2 = I_s e^{-(V_{BE}+V_S)/V_T} = I_1 e^{-V_S/V_T} \tag{2}$$

I_2 flows through Q_5 and Q_{10} as well. Considering Q_{10}, and Q_9 base-emitter voltages can be expressed from the exponential relationship:

$$V_{BE}\big|_{Q_{10}} = -V_T \ln(\frac{I_2}{I_s}) = V_{BE} + V_S \tag{3}$$

$$V_{BE}\big|_{Q_9} = V_T \ln(\frac{I_1}{I_s}) = V_{BE} \tag{4}$$

Therefore, V_2 can be expressed as a function of sensing voltage (V_S),

$$V_2 = -V_{BE}\big|_{Q_{10}} - V_{EE} = -V_{BE} - V_S - V_{EE} \tag{5}$$

Similarly,

$$V_1 = -V_{BE}\big|_{Q_9} - V_{EE} = -V_{BE} - V_{EE} \tag{6}$$

Then, the voltage difference of V_1 and V_2 results in

$$V_1 - V_2 = V_S \tag{7}$$

From the small signal point of view V_2 contains AC waveform directly proportional to the resonant current. Since the voltage switches between zero and positive rail voltage, the

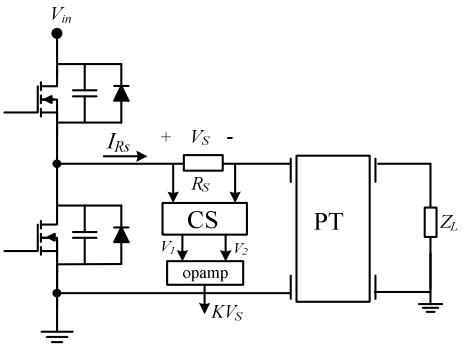

Fig. 1. Block diagram of PT-based switch mode power supply employing current sensing technique with sensing resistor.

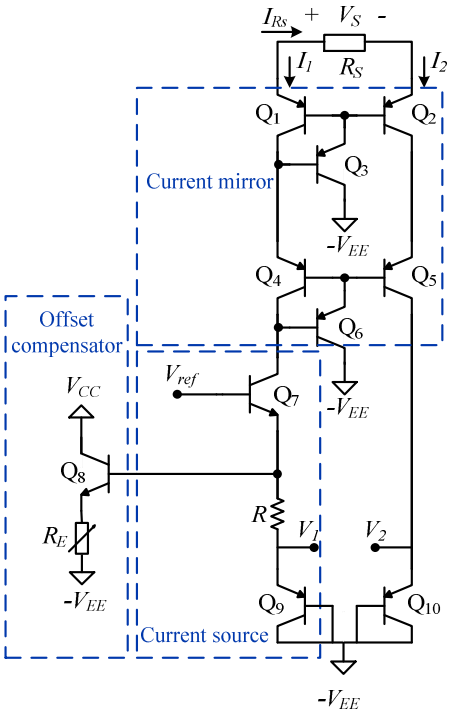

Fig. 2. Schematic circuitry of bi-directional current sensor, operating with the high common mode voltage and wide range of frequency bandwidth.

collectors of both Q_9 and Q_{10} are supplied from a negative voltage ($-V_{EE}$) to provide sufficient voltage headroom for Q_1–Q_9 when the low side switch is turned on (input voltage close to zero). Transistor Q_8 and the variable resistor R_E are inserted to allow an offset compensation for the differential output voltage V_1-V_2. The current drawn in the base of Q_8 can be adjusted by R_E. This changes the current passing through resistor R and consequently allows regulation of DC voltage level of V_1. This, results in zero offset voltage to the differential input of the op amp (Fig. 1).

With ideal matching of Q_7 and Q_8, R_E should be equal to R in order to have the same base current in Q_7 and Q_8 so that the base current in Q_8 compensates for the extra current in R caused by the base current of Q_7. However, in practice some mismatch must be expected, so R_E is made variable to allow an adjustment of the compensating current. Transistors Q_3 to Q_7 should be able to tolerate approximately the input common mode voltage across their collector-emitter. DC supply voltages V_{CC} and V_{ref} are considered as positive and negative voltages, respectively in order to set biasing of Q_7 and Q_8.

A differential op amp can be used as a stage after the current sensor to convert the voltage difference between points V_1 and V_2 into an analog single ended ground-referenced voltage.

B. Design consideration

The value of the sense resistor is determined to be optimum in order to minimize power losses caused by this measurement, which is recommended to be selected as low value (R_s<1Ω) [3]. In some cases, hard switching might occur; therefore switching noises are also passing through R_s. A 100 mΩ sense resistor is considered to be put in series with the primary side of the PT to measure the current in order to obtain a measurable voltage drop (Vs) up to 100 mV across R_s. The AC signal voltage of V_2 should be of the sufficient magnitude to be above the noise floor and can be fed into op amp. Furthermore, the current passing through Q_1 is constant and should be adjusted to a value low enough in order not to have significant influence on the measured current.

III. SIMULATION RESULTS

Bipolar transistor pairs have been used for simulation in order to have good matching between the transistors in the current mirror. The transistors employed are NST30010MXV6T1G, PNP matched pair from ON-Semiconductor for Q_1 ,Q_2 and Q_9 ,Q_{10} , KST92 from Fairchild Semiconductor for Q_3 to Q_6 and SMBTA42 from Siemens for Q_7 and Q_8. The current-gain bandwidth product of transistors are minimum 50 MHz. Components are chosen to fulfill the objective of 200 V as input DC voltage.

The circuit has been simulated using PSpice and including Spice models of each transistor. Fig. 3 shows the simulation results which confirm the design theory and functionality of the circuit. In simulation the maximum input voltage of 200 V is considered. The resonant current is considered as a sinusoidal waveform with the amplitude of 1 A and the frequency of 115.9 kHz. The values of parameters are shown in the table I.

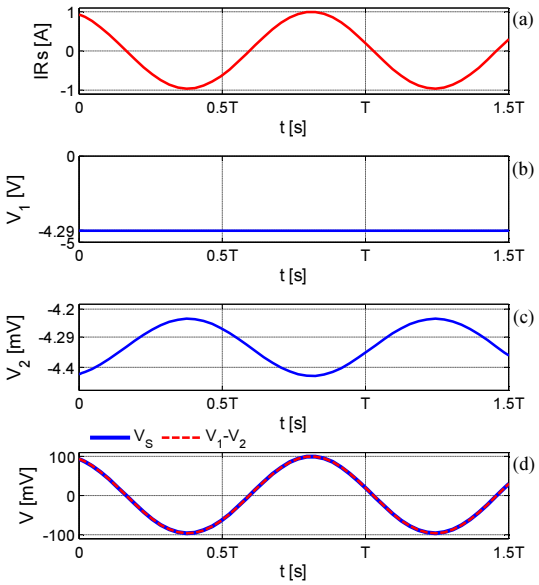

Fig.3. Simulation waveforms, vertical axis of graphs shows current/voltage and horizontal axis shows normalized time; T is the period of 8.628 µs (a) sinusoidal current source; (b) voltage at point V_1; (c) voltage at point V_2 with respect to the ground; (d) output voltage of current sensor with gain of unity compared to the voltage drop across the sensing resistor.

It can clearly be seen that the sensing voltage has been transferred to the voltage V_2 contains DC offset. The output voltage of the current sensor (V_1-V_2) can be adjusted by R_E to have zero DC offset.

As mentioned, one of the design tradeoffs in this resistive current measurement has been selecting the value of the sense resistor to provide sufficient voltage across the base-emitter of Q_2 in order to have large enough voltage value in the output of current sensor. With resistor values larger than 500 mΩ it is easier to measure the voltage difference, since it provides larger voltage to the input of current sensor in low amplitude currents, but it results in dramatic voltage decrease when switches are on.

The functionality of the current sensing circuit has been simulated using the parameters shown in Table I with the current sensing circuit connected to the converter. Mayson's equivalent circuit for a radial mode PT has been used for the simulation. The resonating frequency of this PT is 115.9 kHz. Fig. 4 shows waveforms.

Further circuitry needs to be added to add current waveform at period of the dead time to illustrate the sinusoidal resonant waveform [4].

TABLE I. SIMULATION PARAMETERS

Parameters	Value	Parameter	Value
$-V_{EE}$	-5 [V]	R_E	100 [Ω]
V_{CC}	+5 [V]	R	100 [Ω]
V_{ref}	-3.3 [V]	R_S	100 [mΩ]

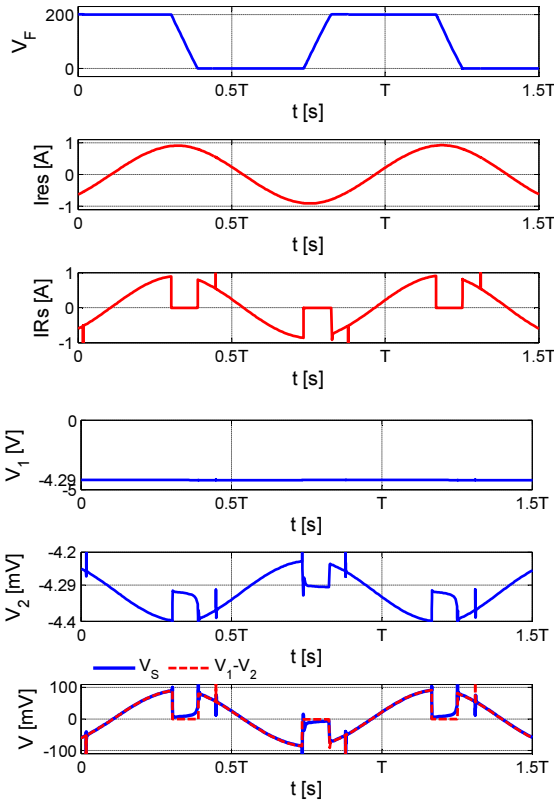

Fig.4. Simulation waveforms, vertical axis of graphs shows current/voltage and horizontal axis shows normalized time, T is the switching period of 8.628 µs; from top: V_F: switching voltage; I_{res}: resonant current; I_{Rs}: current passes through sensing resistor; V_1 and V_2: output voltages of current sensor; V_1–V_2: differential output voltage of current sensor; V_S: sensing voltage.

IV. Conclusion

A new current sensor circuit has been proposed and investigated in this paper. A simple output voltage equation of the proposed circuit is derived. Simulations have demonstrated good agreement with the theoretical predictions.

The proposed circuit has capability to sense differential signal in the presence of a high common mode voltage, which is up to 200 V in this design. This current sensor has general application, even though its functionality has been investigated for a PT-based SMPS. Therefore, the proposed current sensing circuit is suitable for wide range of applications which current needs to be measured in the high voltage line of a SMPS.

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Appendix F

Dynamic optimum dead time in piezoelectric transformer-based switch-mode power supplies

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Accepted for

IEEE Transaction on Power Electronics IEEE-TPEL (2016)

Dynamic optimum dead time in piezoelectric transformer-based switch-mode power supplies

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***Abstract*—Soft switching is required to attain high efficiency in high-frequency power converters. Piezoelectric transformer-based converters can benefit from soft switching in terms of significantly diminished switching losses and stresses. Adequate dead time is needed in order to deliver sufficient energy to charge and discharge the input capacitance of piezoelectric transformers in order to achieve zero-voltage switching. This paper proposes a method for detecting the optimum dead time in piezoelectric transformer-based switch-mode power supplies. The provision of sufficient dead time in every cycle of the switching period results in the quick start up of resonant current inside the transformer. The new method is implemented by dynamically detecting the optimum dead time for each resonant cycle and results in reduced energy loss, and consequently, increased efficiency in the converter during initialization time and steady-state operation. The theory of optimum dead time operation is also discussed in this paper. Experimental results and simulation are provided to show the implementation of the concept.**

***Index Terms*—Optimum dead time; dynamic dead time; switch-mode power supply; zero-voltage switching; piezoelectric transformer.**

NOMENCLATURE

C	Resonant capacitance of the piezoelectric transformer.
C_{d1}	Input electrode capacitance of the piezoelectric transformer.
C_{d2}	Output electrode capacitance of the piezoelectric transformer.
C_{in}	Equivalent input capacitance of the piezoelectric transformer attached to the half-bridge.
C_{oss}	Output capacitance of MOSFETs.
DT	Dead time.
HS	Switching signal driving the high-side switch.
HS_G	High-side gate-drive signal detected by ODT.
i_{res}	The resonant current of the piezoelectric transformer.
I_{pk}	Peak value of the resonant current.
L	Internal inductance of the piezoelectric transformer.
LS	Switching signal driving the low-side switch.
LS_G	Low-side gate-drive signal detected by ODT.
ODT	Optimum dead time.
R	Dielectric losses inside the transformer.
R_m	Matched load for the piezoelectric transformer.
$S(v_F)$	Switching voltage signal scaled to the voltage level of the comparator.
$S_d(v_F)$	Switching voltage signal with a slight delay.
$v_F(t)$	Switching voltage.
V_d	Voltage drop across the body diode of the MOSFETs.
Z_{HS}	Detecting a signal in the output of ODT denotes that the switching voltage has reached the positive rail.
Z_{LS}	Detecting a signal in the output of ODT denotes that the switching voltage has reached ground.
Z_{MH}	Detecting a signal in the output of ODT denotes that the switching voltage has reached the local positive peak.
Z_{ML}	Detecting a signal in the output of ODT denotes that the switching voltage has reached the local negative peak.
Φ_I	Phase shift of the resonant current with reference to the turn-off time of the low-side switch.
Φ_{ODT}	Signal phase corresponding to the optimum dead time.
ω	Switching angular frequency.

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I. INTRODUCTION

The development of piezoelectric transformer (PT)-based switch-mode power supplies (SMPS) has gathered pace in recent times due to their smaller size, lighter weight, lower cost, lower electromagnetic interference (EMI), higher power density, and higher efficiency in comparison with converters used in conventional transformers [1], [2]. Research in this area has yielded devices with greater efficiency by achieving soft switching in PT-based SMPS [1], [3], [4]. In order to obtain zero-voltage switching (ZVS), the dead time (DT) needs to be sufficiently long to allow the input capacitor of the PT to charge or discharge [5], [6]. If the DT is shorter than required, it leads to hard switching; in case the DT is longer, it can lead to hard switching or soft switching with sub-optimal efficiency [7]. Hence, a sufficiently long DT helps reduce power dissipation in switches, and consequently, this increase efficiency [8]–[10].

A fixed DT is allocated for PT-based converters with resistive matched load by analyzing the percentage of the total time required for DT. A few parameters govern the attainment of ZVS under a fixed DT: the rise in temperature, load, and changes in frequency [1], [11]. A drawback of PT-based SMPS with a fixed DT is that the length of DT needs to be separately measured for each transformer because the input capacitor of the PT is different for each transformer,

even those from the same batch of design and production, due to the many parameters involved, e.g., oven temperature and polarization. Therefore, dynamic detection of dead time in PT-based converters is very important.

Several attempts have been made to minimize or eliminate the effect of dead time in power converters [12]–[18]. This effect is known as a distortion of the fundamental output voltage in the voltage source inverters (VSI) in pulse-width modulation (PWM) inverters [12], [13]. The relevant methods have been implemented by detecting the load current in the output of half-bridge switching, which is inapplicable to PT-based SMPS. In PT-based converters, the phase shift in the current is effected by the piezoelectric transformer. Moreover, the input capacitor of the PTs is charged or discharged during the dead time, which renders this situation different from those involving other resonant converters.

This study shows the dependence of ZVS on optional DT in piezoelectric converters, and proposes a method to detect the optimum DT for any type of PT. The outline of the remainder of this study is as follows: Section II is dedicated to a description and analysis of DT and its need in PT-based SMPS. Principle of DT is described in Subsection II-A. Furthermore, the behavior of inductorless, half-bridge, PT-based SMPS is analyzed in Subsection II-B. The idea of optimum DT is introduced in Subsection II-C and compared with prior relevant research. Following this, the implementation of the dynamic DT operation is discussed in Subsections III-A and III-B. Section IV describes experiments and simulation to show the effectiveness of the proposed method in achieving optimum DT. The final section contains the conclusions of this research.

II. Investigation and Analysis of Dead Time in PT-based Converters

A. Principle of dead time (DT)

In SMPS, switches are semiconductors with a built-in delay time. This delay time applies in the gate voltage to drive signal to start up the switching. Typically, the turn-on and turn-off delay times are not equal. Therefore, a certain amount of delay is afforded to the gate drives to prevent the simultaneous turning on of the switches [12]. Therefore, dead time is defined as the interval during a switching transition when both metal-oxide-semiconductor field-effect transistors (MOSFETs) are turned off. The dead time needs to be as short as possible to maintain an accurate low-distortion output signal in audio amplifiers [12], [19], in addition to maintaining a maximum time for switches and reducing energy loss. In PT-based SMPS, converters need to provide reactive energy to the input capacitor of the PT. However, the DT provides an appropriate interval to charge and discharge this input capacitor. In LCC resonant converters, only the output capacitances of the MOSFETs, which are typically on the order of hundreds of picofarads, should be charged by resonant current [4], [20]. However, for PT-based converters, the output capacitors of both MOSFETs and the input capacitor of the PT should be charged by resonant current to raise the voltage from 0 (V) to a positive rail V_{DC}. Fig. 1 shows an inductorless half-bridge

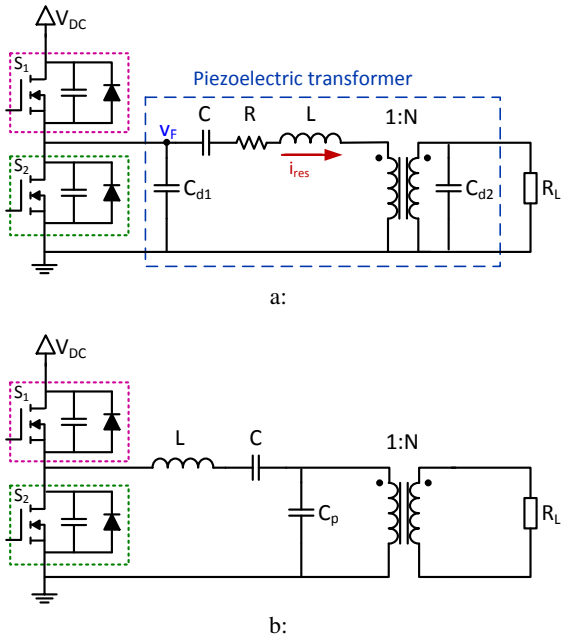


Fig. 1: a: Inductorless PT-based converter; half-bridge topology, b: LCC resonant converter.

PT-based converter [21] and an LCC resonant converter [22]. Since the input capacitance of the PTs are normally in the range of nanofarads, longer time is needed for the resonant current to provide sufficient charge to the capacitors, which means that the DT in PT-based converters is larger than that in LCC resonant converters. The challenge is to keep the DT as short as possible in order to increase efficiency. Furthermore, this will prolong the injection of energy to the transformer during the turn-on time of the high-side switch.

B. Operating modes

In the remainder of this section, the behavior of inductorless PT-based SMPS, when ZVS is attained, is discussed in detail. Eight operating modes divided into four intervals are analyzed, where each of these four intervals consists of two subintervals. Therefore, waveforms in a switching cycle are represented as $t_0 - t_{12}$. Fig. 2 shows both the switching voltage $v_F(t)$ and the resonant current i_{res} waveforms during a switching cycle in the steady state where ZVS is achieved. Time points in Fig. 2 indicate t_0: i_{res} changes direction from positive to negative values; t_2: low-side switch, S_2, is turned off; t_4: $v_F(t)$ reaches the positive rail, V_{DC}; t_5: body diode of the high-side switch, S_1, starts to conduct; t_6: high-side switch, S_1, is turned on; t_{2l}: i_{res} changes direction from negative to positive values; t_8: high-side switch, S_1, is turned off; t_{10}: $v_F(t)$ reaches to the negative rail; t_{11}: body diode of the low-side switch, S_2, conducts; t_{12}: low-side switch, S_2, is turned on. Fig. 3 shows the eight operating modes.

The following analyses are provided based on these assumptions:

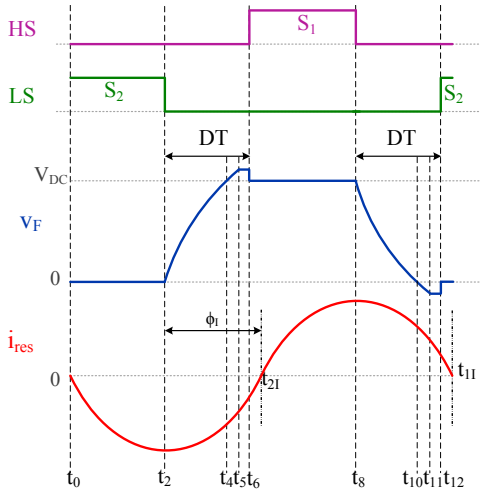


Fig. 2: Steady state switching voltage and resonant current waveforms for inductorless PT-based SMPS where ZVS is achieved.

- The converter's input capacitor is considered a summation of the input capacitance of the PT and the output capacitance of both MOSFETs: $C_{in} = 2\,C_{oss} + C_{d1}$
- Fundamental resonance due to the high quality factor of the PT.

Mason's lumped circuit is used to represent the operation of the converter in terms of resonant current and switching voltage. Resonance current is also shown in order to investigate the operating modes in detail. Since the PT behaves as a high Q-band pass filter, the resonant current is considered as the sinusoidal wave described as:

$$i_{res}(t) = I_{pk}\, sin(\omega t - \phi_I) \tag{1}$$

where I_{pk} is peak of the resonant current, ω is the angular switching frequency, and $\phi_I \in [0, \pi]$ is the current phase angle. The output capacitors C_{oss} of both MOSFET are considered in the input capacitor of the PT, since the parasitic capacitance of MOSFETs is typically considerably lower than C_{d1}. Furthermore, C_{d1} and C_{oss} are charged and discharged together in the DT. Moreover, the DT is studied in detail in this section.

1) S_2 is on: The time interval is $t_{12} - t_2$. The input capacitor of the PT is fully discharged and short-circuited through the low-side switch. At t_{12}, the low-side MOSFET is turned on, and the resonant current freewheels through the low-side switch and changes direction at t_{1I}. A minor difference in voltage occurs across the switch as the low-side switch is turned on. At t_{1I}, the value of the resonant current crosses zero and changes direction from forward to reverse. Therefore, the converter's operation spans across two subintervals. Fig. 3a and Fig. 3b show the equivalent circuit and current flow in this interval, respectively. The following equation represents the switching voltage in this interval:

$$v_F(t) = 0 \tag{2}$$

2) Both switches are off: The subinterval is $t_2 - t_5$. At t_2, the low-side switch is turned off. In this interval, both switches are off, and the resonant current retains its direction in the reverse orientation through the PT input capacitor and charges it to a voltage slightly higher than the DC-link until the diode of the high-side body starts to conduct at t_5. Fig. 3c shows the equivalent circuit and current flow in this interval. The following equation represents the waveform:

$$v_F(t) = \frac{I_{pk}}{C_{in}}\,(cos(\omega t - \phi_I) - cos(\omega t_2 - \phi_I)) + 0 \tag{3}$$

The subinterval is $t_5 - t_6$. At t_5, the high-side body diode starts conducting the reverse resonant current. Therefore, the switching voltage is limited to the sum of the diode voltage and the DC rail voltage. This interval is not required while the PT input capacitor is sufficiently charged for soft switching. Fig. 3d shows the equivalent circuit and the current flow in this interval. The voltage in this interval is expressed as:

$$v_F(t) = V_{DC} + V_d \tag{4}$$

where V_{DC} is the input voltage and V_d is the voltage drop across the body diode of the MOSFETs.

3) S_1 is on: The time interval is $t_6 - t_8$. The high-side MOSFET is turned on. The resonant current freewheels through the high-side switch and is provided to the PT. There occurs a minor voltage difference across the switch as the high-side switch is turned on. At t_{2I}, the resonant current has crossed zero and changes direction from reverse to forward. Therefore, the converter's operation is shown in two subintervals. Fig. 3e and Fig. 3f show the equivalent circuit and the current flow in this interval. The switching voltage is described as:

$$v_F(t) = V_{DC} \tag{5}$$

4) Both switches are off: The time interval is $t_8 - t_{12}$. At t_8, the high-side switch is turned off. In this interval, both switches are off. The resonant current retains its direction in the forward orientation by being fed through the PT input capacitor. Therefore, the PT input capacitor is discharged, and the voltage across approaches a value slightly below zero until the low-side body diode conducts at t_{11}. Fig. 3g shows the equivalent circuit and the current flow in this interval. The switching voltage in this interval is represented as:

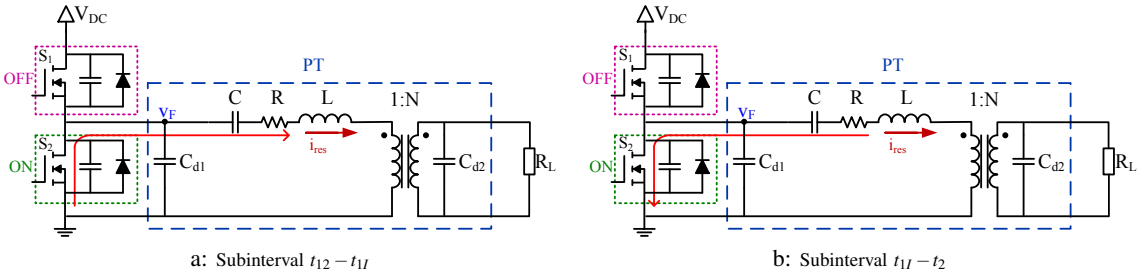
$$v_F(t) = \frac{I_{pk}}{C_{in}}\,(cos(\omega t - \phi_I) - cos(\omega t_8 - \phi_I)) + V_{DC} \tag{6}$$

The time interval is $t_{11} - t_{12}$. At t_{11}, the low-side body diode begins conducting the forward resonant current. Therefore, the switching voltage is limited to a value below zero, which is equal to voltage across the body diode of the MOSFET. This time interval is undesirable while the PT input capacitor is already completely discharged. Fig. 3h shows the equivalent circuit and the current flow in this interval, where

$$v_F(t) = -V_d \tag{7}$$

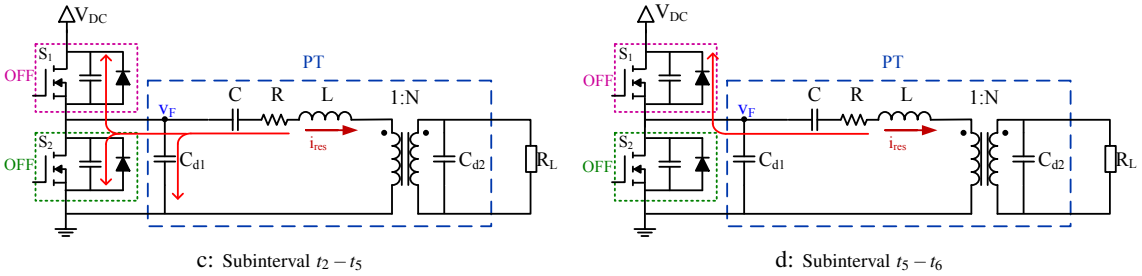
C. Past research and DT optimization

As mentioned in Subsection II-A, it is important to have sufficient DT between the on times of switches. This dead time can generally be shorter or longer than required, which causes hard switching. Fig. 4 shows these situations in the steady state. In order to benefit from soft switching, DT should



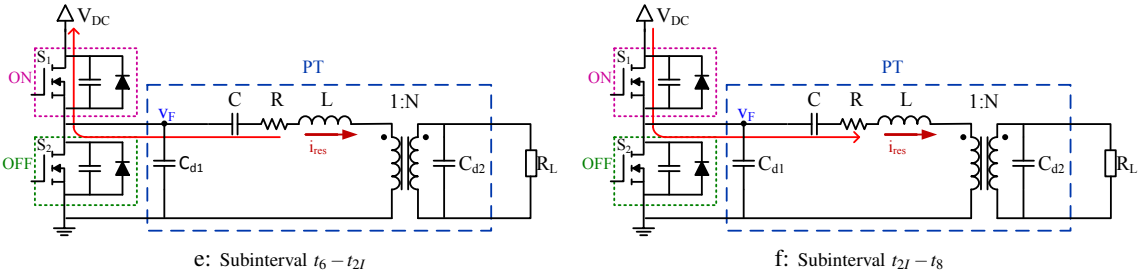
a: Subinterval $t_{12} - t_{1I}$ b: Subinterval $t_{1I} - t_2$

a, b: S_2 is on.



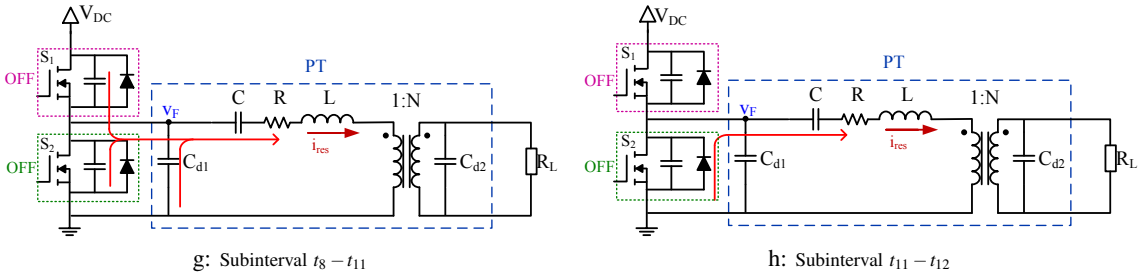
c: Subinterval $t_2 - t_5$ d: Subinterval $t_5 - t_6$

c, d: Both switches are off; transition of voltage from low to high.



e: Subinterval $t_6 - t_{2I}$ f: Subinterval $t_{2I} - t_8$

e, f: S_1 is on.



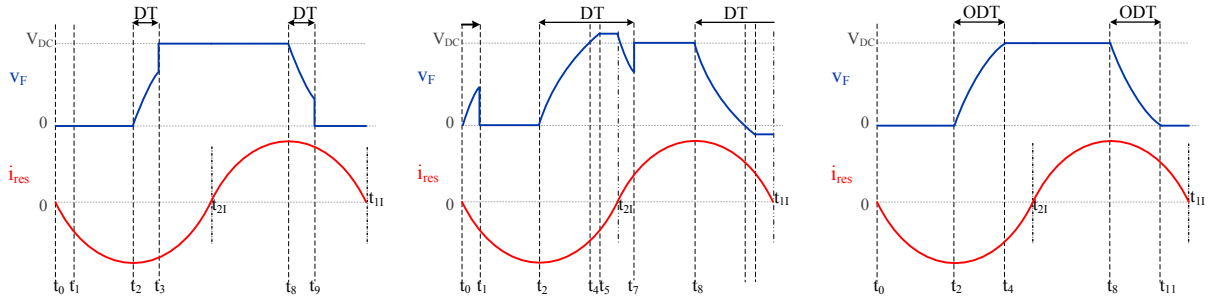
g: Subinterval $t_8 - t_{11}$ h: Subinterval $t_{11} - t_{12}$

g, h: Both switches are off; transition of voltage from high to low.

Fig. 3: Eight general operating modes are described for PT-based SMPS where ZVS is achieved. Mason's equivalent circuit is used for PT.

be properly applied [3].To attain ZVS, the DT should be appropriately considered to charge/discharge the input capacitor of the PT to the positive/negative rails. If switches are turned on before the input capacitor completely charges/discharges, hard switching occurs, as shown in Fig. 4a. Moreover, the case where the DT is longer than required is shown in Fig. 4b. In this case, when the resonant current changes direction, the body diodes do not conduct. Therefore, C_{d1} starts discharging at t_{2I} or charging at t_{1I} before the switches are turned on [23].

In past research, the DT was taken to be a fixed value in order to ensure that the ZVS was obtained in steady-state operation [24]–[27], and is typically sufficient. Moreover, with a fixed DT during initialization, the build up of resonant current is delayed, and it takes longer for the circuit to reach the steady state. The reduction in the start-up time may not be considerable in general, but becomes important when the



a: Insufficient dead time, short b: Insufficient dead time, long c: Optimum dead time

Fig. 4: Steady state: (a) DT is shorter than required, containing 4 operating modes. t_3 and t_9 show turn on time of S_1 and S_2, respectively. (b) DT is longer than required. t_1 and t_7 show turn on time of S_2 and S_1, respectively. (c) Switching voltage and resonant current waveforms following optimization.

converter needs to be frequently turned on and off, e.g., when burst-mode control is used to control the converter's output voltage [25], [28], [29]. In order to avoid both the cases shown in Figs. 4a and 4b and select a sufficiently long DT, the DT is optimized.

The idea implemented in this paper is to optimize dead time. In order to do so, the dead time should be detected and set dynamically in every cycle. In this method of optimization, during each switching cycle, switches are turned on when the switching voltage reaches its minimum or maximum value in start-up time, or when it reaches the positive or negative rails in the steady-state period. Fig. 4c shows waveforms when a converter in the steady state has been optimized.

D. Analysis of optimum DT

This subsection shows the dependence of optimum dead time on the resonant current, which is imposed by the resonant tank of the PT. Therefore, the switching voltage is analyzed during DT. In an inductorless PT-based SMPS, DT is partially dependent on the amount of energy that the resonant tank provides to the input capacitor of the PT [11]. Hence, when both switches are off and the input capacitor of PT starts charging/discharging, the time taken by C_{d1} to reach the rails is dependent on the instantaneous resonant current. In other words, DT is highly dependent on the peak of the resonant current, I_{pk}, and the phase angle, ϕ_I, at which the tank is operated, both of which are dependent on the PT and the load [4]. Fig. 5 shows the switching voltage and the resonant current where the optimum dead time is applied. The reference point for the phase angle is considered when low-side switch is turned off. When the low-side switch is turned off at $t_2 = 0$, negative resonant current passes through the input capacitor of the PT (C_{in}). An equivalent circuit in this operating mode is shown in Fig. 3c. $v_F(t)$ in $t_2 < t < t_4$ is described as:

$$v_F(t) = \frac{I_{pk}}{C_{in}} \left(cos(\omega t - \phi_I) - cos(\phi_I)\right) \tag{8}$$

By implementing ODT, $v_F(t_4) = V_{DC}$ and $\omega t_4 = \phi_{ODT}$, the analysis of ODT yields

$$\phi_{ODT} = \arccos\left(\frac{V_{DC}\, C_{in}}{I_{pk}} + cos(\phi_I)\right) + \phi_I \tag{9}$$

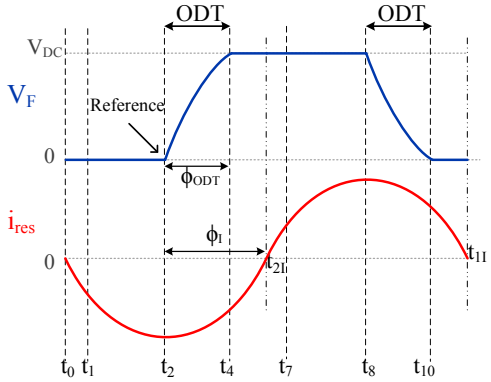


Fig. 5: Switching voltage and resonant current with ODT.

where $\phi_{ODT} \in [0, \pi]$. The dependence of the ODT on resonant current (I_{pk} and ϕ_I) shows that it is difficult to analytically calculate the ODT, even for a specific PT and a specific load. However, the amplitude of the resonant current and its phase angle varies with the temperature of the PT [30]. The method proposed in this paper to detect the ODT is a simple solution that works by varying the temperature and load of the PT.

III. Optimum Dead Time (ODT)

A. Dynamic DT operation

As shown in Fig. 2, there are two DT periods in each switching cycle corresponding to time intervals $t_2 - t_6$ and $t_8 - t_{12}$, as described in Subsection II-B. Having two subintervals $t_2 - t_4$ and $t_8 - t_{10}$ is necessary in order for the voltage to reach across C_{d1} to the rails to attain ZVS. In effect, optimum DT is defined as the minimum time required for the switching voltage ($v_F(t)$) to reach from one DC rail voltage to another. Therefore, by detecting time points where the switching voltage reaches zero and the positive rails, time intervals $t_4 - t_6$ and $t_{10} - t_{12}$ can be reduced to the minimum possible. On the contrary, optimizing time intervals $t_2 - t_4$ and $t_8 - t_{10}$ occurs by detecting t_4 and t_{10}, shown in Fig. 2, in order to turn on the high-side and low-side switches at these time points, respectively. This yields optimum dead time. The ODT leads to a quick start up of the resonant current by maximizing the on time of switches to

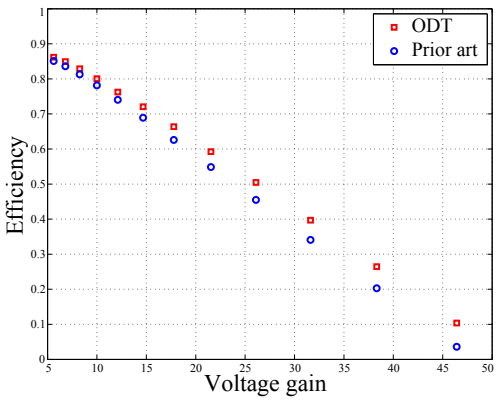


Fig. 6: Efficiency increment by applying ODT for the step-up converter with capacitive load compated to the past research [25], [26].

energize the resonant tank and build up the resonant current. This consequently increases the converter's efficiency.

Improvement in efficiency by applying the ODT for the step-up converter with a capacitive load is shown in Fig. 6. Fig. 7 shows the DT period by waveform and an equivalent circuit of the inductorless PT-based converter. The load was considered the PT's resistive matched load with the relation

$$R_m = \frac{1}{\omega C_{d2}} \tag{10}$$

In a DT interval, the PT's input capacitor was charged/discharged. In order to obtain the shortest period for switching voltage $v_F(t)$ to reach the DC-link in the DT interval, a novel idea was proposed and implemented in this paper. For example, the DT interval during which C_{in} is charged $(t_2 - t_6)$ is explained in detail. At the start of the DT interval, the resonant current has a negative value but its amplitude is dependent on the phase shift imposed by the transformer. For simplicity of understanding, the best case is explained in this section in detail, where $\phi_I = \pi/2$. If $ODT > \pi/2\omega$, the resonant current changes its direction from negative to positive, and causes the discharge of C_{in} in order to provide energy back to the resonant tank, as shown in Fig. 7e. If the energy of the resonant tank is supplied through the DC-link by turning on the high-side switch, it prevents C_{in} from being discharged (Fig. 7f). If C_{in} is not discharged in $t_2 - t_6$ or charged in $t_8 - t_{11}$,

- Lower switching losses, since $\Delta V_{F_b} < \Delta V_{F_a}$. This results in higher efficiency.
- More energy injected to the PT for the build up of the resonant current to reach the steady state. This causes resonant current of higher amplitude in each cycle as well as shorter start-up time. The following shows the parameterized energy saved by applying ODT:

$$\Delta E = \Delta E_b - \Delta E_a \tag{11a}$$

where,

$$\Delta E_b = \frac{1}{2} C_{in} V_{DC}^2$$

$$\Delta E_a = \frac{I_{pk}^2}{4 C_{in}} \left[\Delta DT + \frac{1}{2} sin(2\Delta DT) \right] \tag{11b}$$

B. Implementation of the proposed method

By measuring input voltage of the PT and comparing it with the rail voltages (zero/positive), the switches should be turned on, which is satisfactory for the steady-state period. The start up time or the initialization time specifies the period from when the converter turns on to when the resonant current in the PT reaches the maximum amplitude in its operating point. In this period, the resonant current increases continuously but does not reach the highest possible amplitude. Therefore, the input capacitor is not charged up to the positive rail or discharged down to zero. Fig. 9 shows the states that may occur for the voltage and current waveforms in the initialization period. Accordingly, the two states may occur during the DT in the start up. In one case, the switching voltage may pass through the local maximum/minimum before switches are turned on. Fig. 9b shows the switching voltage and the resonant current for this case. Extrema occur in $v_F(t)$ because the resonant current changes its direction during the dead time. Therefore, it causes the input capacitor to charge and discharge.

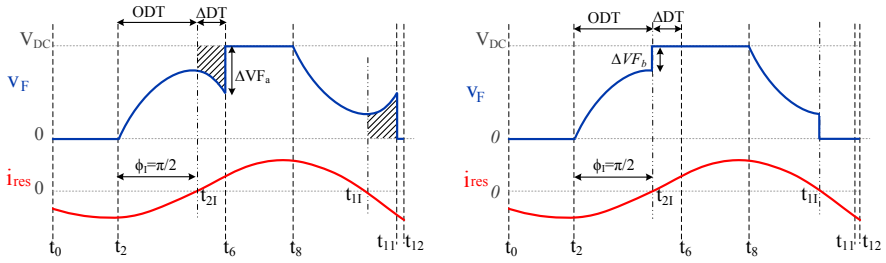
In the other case, the switching voltage continues to increase/decrease until the switches are turned on. This means that the switching voltage will not pass through any local extrema. In this case, the amplitude of the resonant current is not sufficiently high to charge the input capacitor. This situation is shown in Fig. 9a. In the meantime, the resonant current changes direction during a switching cycle. The difference between the cases, which may originate in the start-up period, is the amplitude of the resonant current. The resonant current starts to build up once the converter is turned on, and grows in amplitude until it reaches the steady state. In the steady state, the amplitude of the resonant current is constant under the same conditions, i.e., input voltage, temperature, and load. At the beginning of the initial period, the amplitude of the resonant current is very low. Hence, there is insufficient energy injected into the input capacitor of the PT during the dead time to charge the C_{in} to the DC-link voltage. Both cases are shown in Fig. 9a and Fig. 9b. The best condition for the charge of C_{in} is shown in Fig. 9c, where the resonant current is near its peak when the dead time starts, and this means that $\phi_I = \pi/2$ is related to $t_2 = 0$. Therefore, $v_F(t)$ can be simplified as:

$$v_F(t) = \frac{I_{pk}}{C_{in}} sin(\omega t) \tag{12}$$

Consequently, the total amount of energy provided to C_{in} during dead time is defined as $\Delta t = t_6 - t_2$.

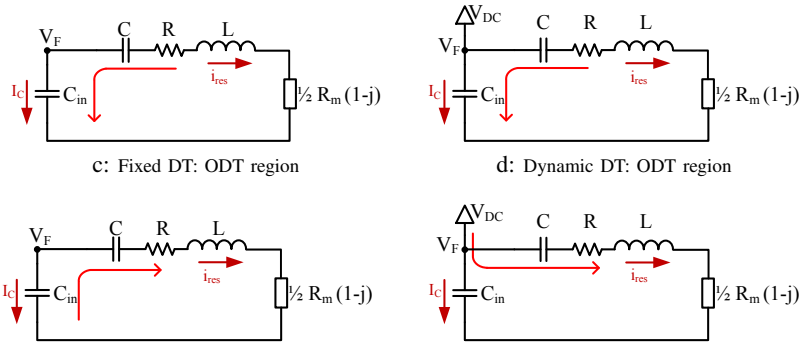
$$\Delta E = \frac{1}{2} C_{in} V_{F(rms)}^2 |_{\Delta t} = \frac{I_{pk}^2}{4 C_{in}} (1 - \frac{1}{2\omega\Delta t} sin(2\omega\Delta t)) \tag{13}$$

Therefore, it is important to turn on switches at the zero crossing of the resonant current, as shown in Fig. 9c. Consequently, in order to optimize dead time either in the initialization state or in the steady state, switches should be turned on when the switching voltage reaches the rails (positive/ zero) or resonant current crosses zero. If none of these signals are detected, the



a: Fixed DT b: Dynamic DT

a, b: Resonant current and switching voltage waveforms.



c: Fixed DT: ODT region d: Dynamic DT: ODT region

e: Fixed DT: ΔDT region f: Dynamic DT: ΔDT region

c, d, e, f: Equivalent circuits in DT interval for case a: (c and e) and case b: (d and f); R_m is matched load.

Fig. 7: Effect of dynamic dead time in reducing requisite input energy and switching losses in initialization time.

circuit applies a fixed DT to facilitate the build up of resonant current. Since there is no direct access to the resonant current inside the PT, the switching voltage is used as a reference for detecting the DT in this implementation. Table I shows both cases during the initialization period. Fig. 8 shows a block diagram of the converter used in this paper. Outputs of the ODT block determine turn on time of the high-side and low-side switches.This contribution is performed dynamically by mix of analog and digital control techniques used in digital block and programming done in field-programmable gate array (FPGA). FPGA is used for implementation of control techniques to generate high-side and low-side gate voltages based on the detected signals in the output of the ODT block.

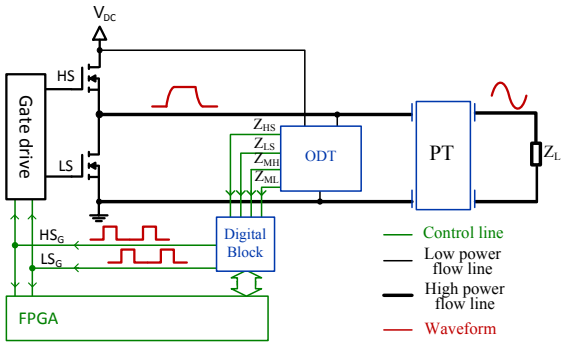
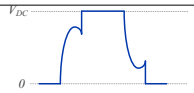
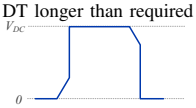
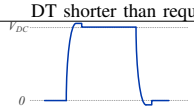
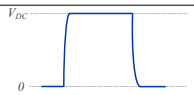


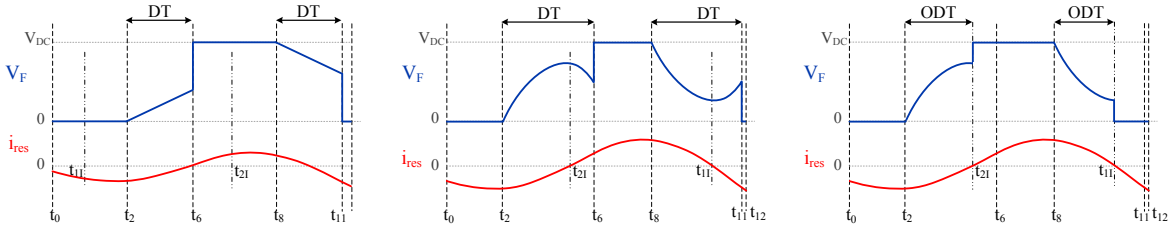
Fig. 8: Block diagram of converter with ODT and mix of analog and digital control techniques through digital block and FPGA.

C. ODT circuit description

Fig. 10 shows a circuit block diagram of the implemented optimum DT. The circuit consists of two parts: the "steady state ODT detector" detects the ODT in the steady state, and the "extrema detector" identifies the ODT during the initialization period. For the steady state, the switching voltage is compared to the positive DC-link (V_{DC}) and the zero line through op-amps 1 and 2. This results in Z_{HS} and Z_{LS} in the output of the ODT block. Therefore, the high- and low-side switches are turned on by raising the edges of Z_{HS} and Z_{LS} in the steady state. For the initialization period, the switching voltage taken as the input signal S is compared with its delayed S_d. The local maximum is detected when $S_d > S$ and the local minimum is detected when $S > S_d$. A voltage range called the middle range (M) is defined between V_{Low} and V_{Hi}. It is considered 10% and 90% of V_{DC}, respectively, in order to define a margin for local extrema detection. This also prevents the influence of noise in extrema detection. Op-amps 3 and 4 determine whether the $v_F(t)$ is above V_{Low} or below V_{Hi}. The amplitude of $v_F(t)$ is scaled down and called as signal S. A high-precision dual output comparator is used to compare $v_F(t)$ known as signals S with its delayed signal S_d. The outputs of the ODT block are controlled by the digital block. The high-side MOSFET is turned on when Z_{HS} or Z_{MH}

TABLE I: SWITCHING VOLTAGE COMPARISON BETWEEN PAST RESEARCH AND OPTIMUM DEAD TIME METHOD

State	Prior art	Optimum dead time
Initialization time	 DT longer than required  DT shorter than required	 Sufficient DT
Steady state	 Sufficient DT; not optimized	 Sufficient DT



a: Fixed dead time b: Fixed dead time c: Optimum dead time

Fig. 9: Start-up period with fixed DT for (a) and (b). Switching voltage does not reach the rails. The resonant current is low in amplitude. (a) The PT's input capacitor charges/discharges slowly. (b) $v_F(t)$ reaches a local extrema. (c) The ODT is applied to the start up to detect extrema.

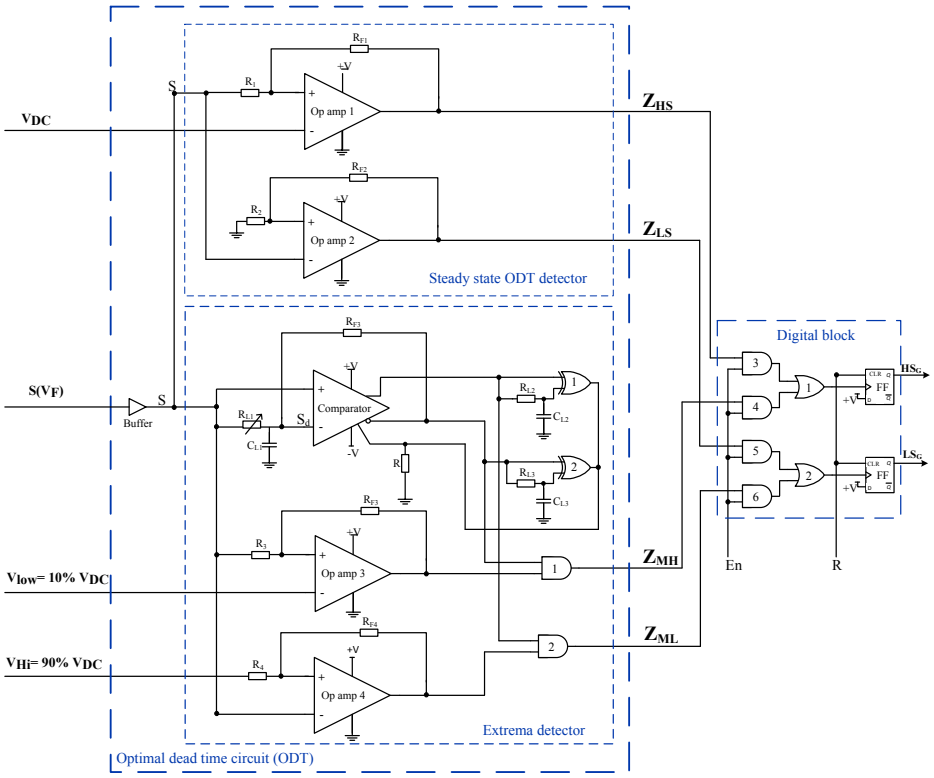


Fig. 10: Circuit block diagram of ODT.

TABLE II: SWITCHING TURN ON TIME POINTS

	Prior art	Optimization
Start up time	Fixed DT	Switching voltage reaches its extrema
Steady state	Fixed DT	Switching voltage reaches the rails

digitally becomes '1', and the low-side MOSFET is turned on when Z_{LS} or Z_{ML} becomes '1'. The control signal reset "R" turns off the switches once the allocated on time ends. However, "En" enables/disables the contribution of the ODT to the converter. Voltages V_{DC}, V_{Hi}, and V_{Low} are scaled to the voltage level of the comparator's input. The Boolean functions implemented for the outputs of the ODT are:

$$\begin{cases} Z_{ML} = (S < V_{Hi}) \cdot (S > S_d) \\ Z_{MH} = (S > V_{Low}) \cdot (S < S_d) \\ Z_{HS} = (S > V_{DC}) \\ Z_{LS} = (S < 0) \end{cases} \tag{14}$$

$$\begin{cases} HS_G = (Z_{HS} + Z_{MH}) \cdot En \cdot \overline{R} \\ LS_G = (Z_{LS} + Z_{ML}) \cdot En \cdot \overline{R} \end{cases} \tag{15}$$

Furthermore, the functionality of the ODT block is shown through waveforms both in the steady state and the start-up time. Fig. 11 shows the signal waveforms in the start-up period related to Fig. 9c. Fig. 12 shows the signal waveforms for the steady state related to Fig. 4c.
Table I compares the ODT with the results of past work by providing a demonstration of switching voltage waveforms both during start up and in the steady state. Table II compares the switching voltage values from past research and the ODT.

IV. Results

The experiments and simulation to establish the effectiveness of the proposed method were carried out by using a radial-mode piezoelectric transformer shown in Fig. 13, and with an equivalent circuit shown in Fig. 1a. The parameter values of the PT are shown in Table III. The PT resonant frequency was 116.3 kHz for the simulation with a resistive load of 300 Ω.Fig. 14 shows the simulation results in start-up transient time both for prior art [25] and for optimization state. By implementing optimum DT, a shorter initialization time was achieved in comparison with the results of past work. The top subfigure of Fig. 14 shows the result for a fixed DT chosen very close to the ODT in the steady state. The selected fixed DT shows almost the best case of setting the DT in past work in the area. The switching voltage V_F reaches the positive rail in the eighth cycle. The bottom subfigure shows the simulation results by applying dynamic DT to each switching cycle. The switches are turned on by detecting the extrema of the switching voltage during start up. The switching voltage reaches the positive rail in the sixth cycle. A comparison of these two cases establishes the idea that the converter reaches the steady state more quickly by applying the ODT. Fig. 15 shows the board that was designed and used for the experiment.

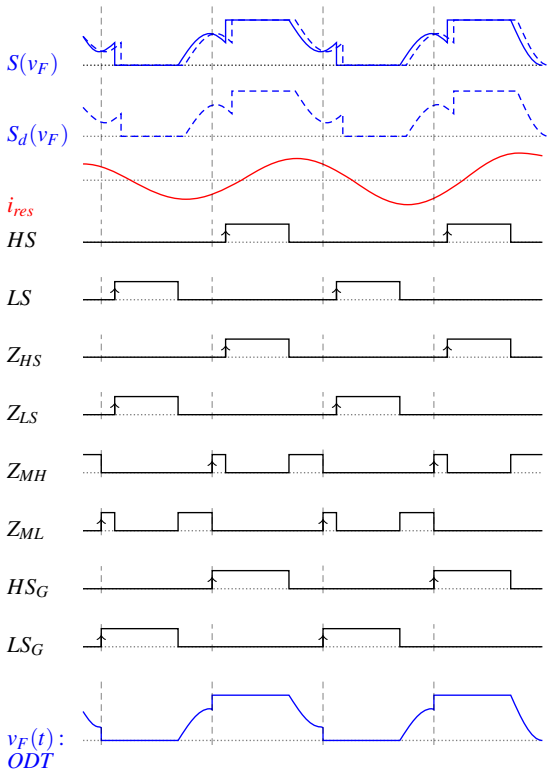


Fig. 11: Signal waveforms, in the start-up, Z_{MH} and Z_{ML} turn on the S_1 and S_2 switches, respectively.

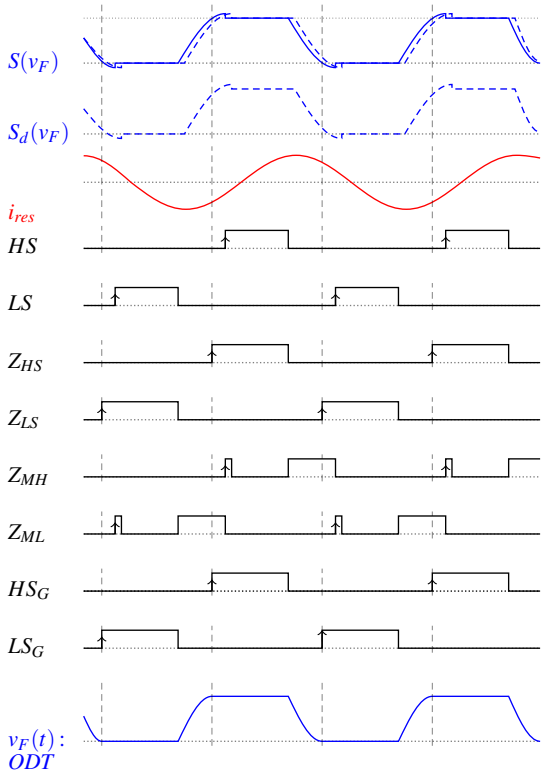


Fig. 12: Signal waveforms, in the steady state when ZVS is achieved; Z_{HS} and Z_{LS} turn on the S_1 and S_2 switches, respectively.

TABLE III: PT EQUIVALENT PARAMETERS

Parameter	Value	Parameter	Value
C_{d1}	3.8 nF	C_{d2}	626 pF
C	565 nF	R	5.6 Ω
L	3.5 mH	N	3.5

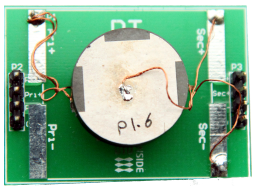


Fig. 13: The Radial-mode piezoelectric transformer used in experiments.

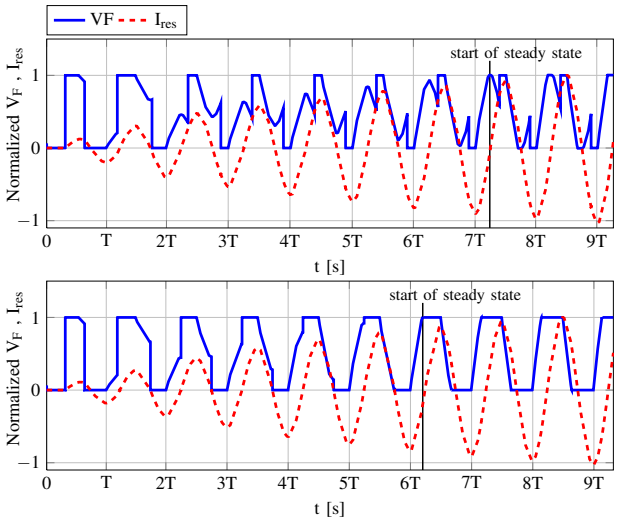


Fig. 14: Start-up period: Comparison of results of past work (top plot) with a fixed DT with the ODT (bottom plot). The driver reaches the steady state faster with ODT than previously proposed methods.

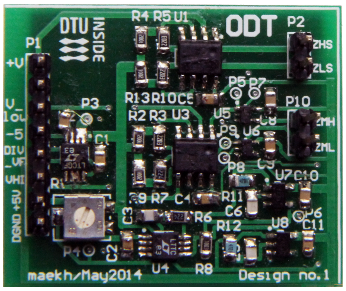
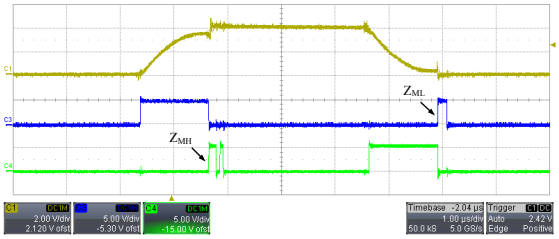
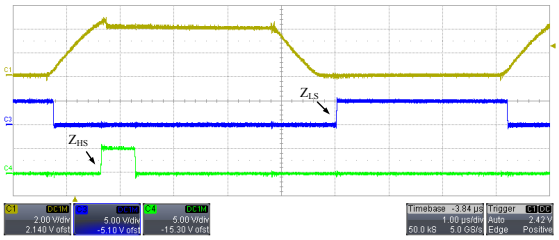


Fig. 15: ODT board used for experiments.



a: Local minimum/maximum detection of switching voltage ($v_F(t)$) in the start-up period or when hard switching occurs; C1: switching voltage $v_F(t)$, C3: local minimum detector by signal Z_{ML}, C4: local maximum detector by signal Z_{MH}.



b: Switching voltage $v_F(t)$ in the steady state or when soft switching occurs. C1: switching voltage $v_F(t)$, C3: negative rail detector by signal Z_{LS} , C4: positive rail detector by signal Z_{HS}.

Fig. 16: Outputs of ODT block by detecting optimum dead time.

Fig. 16 shows the experimental results. In the result shown, input voltage is 4 V with a load of 300 Ω. The measurement is done in low voltage due to limitation of PT in terms of its power transfer capability. The implementation can be used for every input voltage if the desired power can be put through the PT. Fig. 16a shows waveforms at 118.7 kHz, when the ODT block detected an extrema, and Fig. 16b shows waveforms at 119.2 kHz, when the switching voltage reached the rails. A slight delay can occur from the time when the ODT is detected until the switches are turned on due to propagation delay in the gate driver. This time delay can be reduced by selecting a gate driver with lower propagation delay. In this setup, the propagation delay of the gate driver was 35 ns.

V. Conclusion

This paper dealt with the theory of dead time along with its necessity in resonant converters, particularly in inductorless PT-based SMPS. Moreover, the importance of selecting an appropriate dead time in order to avoid hard switching was explained. A new method was proposed and implemented to detect the optimum dead time in PT-based SMPS. However, this method can generally be used for any PT-based converter, even though it is implemented in an inductorless PT-based SMPS. The optimum dead time is obtained at any switching frequency and is updated during every cycle. Detecting the optimum dead time yields two advantages for power converters: reducing the start-up time of the converter in transient operation, and maximizing the turn-on time of switches in the steady state. Furthermore, experimental results and a simulation verified the effectiveness of the proposed method. The ODT is used due to its effective build up of resonant current through an optimized start up, minimization of dead time, the outstanding performance of the ZVS, and energy conservation during initialization. This results in greater efficiency.

A major disadvantage of using ODT is its complex control method, since an additional ODT block is required to be added to the converter. Furtheremore, mixed analog and digital control techniques are needed to impose output signals of the ODT block into the gate voltages in every switching cycle.

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Appendix G

Resonant power converter comprising adaptive dead-time control

Patent application, DTU-95633/P1758EP00 (June 2015)

Inventors: Marzieh Ekhtiari, Thomas Andersen, Tiberiu-Gabriel Zsurzsan

RESONANT POWER CONVERTER COMPRISING ADAPTIVE DEAD-TIME CONTROL

The invention relates in a first aspect to a resonant power converter comprising: a first power supply rail for receipt of a positive DC supply voltage and a second power supply rail for receipt of a negative DC supply voltage. The resonant power converter comprises a resonant network with an input terminal for receipt of a resonant input voltage from a driver circuit. The driver circuit is configured for alternatingly pulling the resonant input voltage towards the positive and negative DC supply voltages via first and second semiconductor switches, respectively, separated by intervening dead-time periods in accordance with one or more driver control signals. A dead-time controller is configured to adaptively adjusting the dead-time periods based on the resonant input voltage.

BACKGROUND OF THE INVENTION

A sub-group of resonant power converter comprises a piezoelectric transformer as a resonant circuit or resonant tank. Piezoelectric power converters are a viable alternative to traditional magnetics based resonant power converters in numerous voltage or power converting applications such as AC/AC, AC/DC, DC/AC and DC/DC power converter applications. Piezoelectric power converters are capable of providing high isolation voltages and high power conversion efficiencies in a compact package with low EMI radiation. The piezoelectric transformer is normally operated in a narrow frequency band around its fundamental or primary resonance frequency with a matched load coupled to the output of the piezoelectric transformer. The optimum operating frequency or excitation frequency shows strong dependence on different parameter such as temperature, load, fixation and age. So-called zero-voltage-switching (ZVS) operation, or soft-switching, of a driver circuit, coupled to the input terminal of a resonant network, which may comprise a piezoelectric transformer, may be achieved via the intrinsic input impedance characteristics of the resonant network or may be achieved by coupling an external inductor in series or parallel with the output signal supplied by the driver circuit. In both cases an input impedance of the resonant network may appear inductive across a relatively large frequency range such that capacitances at the output of the driver circuit can be alternatingly charged and discharged by resonant current during dead-time periods of

the driver circuit without inducing prohibitive power lossess. The driver circuit may comprise a half-bridge or full-bridge MOS transistor circuit.

For obtaining the desired zero voltage switching (ZVS), a dead-time period or interval (DT) of the driver circuit needs to be sufficiently large to allow charging and discharging of the input terminal of the resonant network. The present inventors have discovered that a dead-time period shorter than required for zero voltage switching causes hard switching of the driver circuit. Likewise, a dead-time period longer than required for zero voltage switching may either cause hard switching of the driver circuit or may cause soft switching of the driver circuit with sub-optimum efficiency. However, prior art resonant power converters have been provided with a fixed dead-time period, for example tailored to characteristics of a particular piezoelectric transformer at fixed operating conditions. The fixed dead-time period is unable to account for manufacturing tolerances and drift of active and passive electronic components of the resonant power converter, in particular those of a piezoelectric transformer. Hence, the use of fixed dead-time period leads to increased power consumption of practical resonant power converters where the above-mentioned manufacturing tolerances and drift of active and passive electronic components are inevitable.

Hence, it would be advantageous to provide adjustable dead-time periods of appropriate length or duration to secure zero voltage switching of the driver circuit of a resonant power converter in general and in piezoelectric power converters specifically.

SUMMARY OF THE INVENTION

A first aspect of the invention relates to a resonant power converter comprising:
a first power supply rail for receipt of a positive DC supply voltage and a second power supply rail for receipt of a negative DC supply voltage,
a resonant network comprising an input section and an output section wherein the input section comprises an input terminal for receipt of a resonant input voltage and the output section comprises an output terminal for providing a resonant output voltage in response to the resonant input voltage,
a driver circuit comprising a first semiconductor switch coupled to the positive DC supply voltage and a second semiconductor switch coupled to the negative DC sup-

ply voltage and a driver output connected to the input terminal for supply of the resonant input voltage;

wherein the driver circuit is configured for alternatingly pulling the resonant input voltage towards the positive and negative DC supply voltages via the first and second semiconductor switches, respectively, separated by intervening dead-time periods in accordance with one or more driver control signals,

a dead-time controller configured to adaptively adjusting the dead-time periods based on the resonant input voltage.

The dead-time controller is able to provide adequate length or duration of the dead time periods of the driver circuit to deliver sufficient energy for charging and discharging the input capacitance at the input terminal of the resonant network for example an input electrode of a piezoelectric transformer. This feature enables zero voltage switching (ZVS) and/or zero current switching (ZCS) of the driver circuit and minimizes the energy consumption involved in the switching activity of the first and second semiconductor switches of driver circuit. The dead-time controller of the resonant power converter may utilize various features of the resonant input voltage for detecting an optimum dead time period and adaptively adjusting the dead-time period. The dead-time controller may be configured to adjust the dead-time period during every switching cycle of the resonant input voltage based on an instantaneous value thereof. The switching cycle is determined by a switching frequency of the resonant power converter. Alternatively, the dead-time controller may be configured to adjust the dead-time period during a specific operating condition of the power converter for example solely during a start-up phase or initialization time of the resonant network or solely during steady state operation of the resonant network as discussed in further detail below with reference to the appended drawings. The adaptive adjustment of the dead-time period may hence result in a decrease of energy loss and consequently increased efficiency of the resonant power converter both during the start-up phase and during steady state operation.

If the resonant network comprises a piezoelectric transformer which may possess a zero-voltage-switching factor (ZVS factor) larger than 100%, preferably larger than 120%, such as larger than 150% or 200%. This means the piezoelectric transformer possesses native ZVS properties or characteristics as discussed in further detail for

example in U.S. patent application No. 14/237,432. A number of highly useful piezoelectric transformers suitable for application in the present piezoelectric power converters with high power conversion efficiencies and native ZVS properties are disclosed in European patent application No. 11176929.5.

The driver circuit may comprise a half-bridge or H-bridge driver. The half-bridge driver circuit may comprise a first semiconductor switch and a second semiconductor switch coupled in series between the positive DC supply voltage and the negative DC supply voltage. A midpoint node between the first and second semiconductor switches may be deliver the driver output voltage or signal to the input terminal of the resonant network such as an input electrode or electrodes of a primary/input section of the piezoelectric transformer. Each of the first and second semiconductor switches may comprise a MOSFET for example a DMOS, PMOS or NMOS device. Each of the first and second semiconductor switches further comprises a control terminal or input such as a gate terminal for receipt of the driver control signal. A first driver control signal of the first semiconductor switch is configured to switch the first semiconductor switch between a conducting/ON state and a non-conducting/OFF state. A second driver control signal of the second semiconductor switch is likewise configured to switch the second semiconductor switch between a conducting/ON state and a non-conducting/OFF state. The first and second driver control signals are preferably non-overlapping such that the first semiconductor switch pulls the resonant input voltage towards the positive DC supply voltage via its relatively small on-resistance in the conducting state and the second semiconductor switch after the intervening dead-time period pulls the resonant input voltage towards the negative DC supply voltage via its relatively small on-resistance in the conducting state. Hence, during the dead time period the resonant input voltage or signal is alternatingly charged and discharged from the positive DC supply voltage to the negative DC supply voltage and vice versa by resonant current flowing through an intrinsic input impedance of the piezoelectric transformer and/or by resonant current flowing through, or out of, a series inductor of the resonant network as discussed in further detail below with reference to the appended drawings. The resonant input signal is clamped to the positive DC supply voltage in a first time period where the first semiconductor switch is conducting and the second semiconductor switch non-conducting. Likewise, the resonant input signal is clamped to the negative DC sup-

ply voltage in a second time period where the second semiconductor switch is conducting and the first semiconductor switch non-conducting.

Hence, according to one embodiment of the resonant power converter, the first semiconductor switch comprises a conducting state where the input terminal is connected to the positive DC supply voltage and the second semiconductor switch comprises a conducting state where the input terminal is connected to the negative DC supply voltage; and where the first semiconductor switches is in a non-conducting state during the dead-time periods and the second semiconductor switch is in a non-conducting state during the dead-time periods.

The switching frequency of the resonant power converter may lie between 75 kHz and 500 kHz such as between 100 kHz and 150 kHz. The resonant power converter may comprise a feedback loop which induces self-oscillation of the resonant power converter. The feedback loop ensures that the switching or excitation frequency automatically tracks changing characteristics of a piezoelectric transformer and electronic circuitry of the input side of the power converter.

According to one embodiment, the dead-time controller utilizes a level or amplitude of the instantaneous resonant input voltage to detect the respective time instant to switch the first or the second semiconductor switch to its conducting state. According to another embodiment, the dead-time controller utilizes a waveform shape of the instantaneous resonant input voltage to detect the respective time instants or phases at which to switch the first or second semiconductor to the conducting state as discussed in further detail below with reference to the appended drawings.

The dead-time controller may be configured to adjust a phase or timing of the first driver control signal of the first semiconductor switch and a phase or timing of the second driver control signal of the second semiconductor switch to adaptively adjust the duration of the dead-time periods as discussed in further detail below with reference to the appended drawings.

The dead-time controller may comprise a steady-state controller comprising:
a first comparator configured to compare the instantaneous resonant input voltage

to the positive DC supply voltage and supply a first comparator output signal (Z_{HS}) for adjusting the phase of the first driver control signal in accordance with the first comparator output signal. A second comparator of the steady-state controller may be configured to compare the instantaneous resonant input voltage to the negative DC supply voltage and supply a second comparator output signal (Z_{LS}) for adjusting the phase of the second driver control signal in accordance with the second comparator output signal.

The dead-time controller may comprise a start-up controller configured to detect a waveform shape of the instantaneous resonant input voltage; and
generating a first control signal (Z_{MH}) for adjusting the phase of the first driver control signal in accordance with the waveform shape; and/or
generating a second control signal (Z_{ML}) for adjusting the phase of the second driver control signal in accordance with the waveform shape.

The dead-time controller may be configured to detect the waveform shape of the resonant input voltage by comparing the instantaneous resonant instantaneous transformer input voltage with a delayed replica of the resonant input voltage as discussed in further detail below with reference to the appended drawings. The waveform shape of the resonant input voltage may be utilized by the dead-time controller to:
detect a local maximum of the waveform of the instantaneous resonant input voltage in response to the delayed replica of the resonant input voltage exceeds the instantaneous resonant input voltage; and/or
detect a local minimum of the waveform of the instantaneous resonant input voltage in response to the delayed replica of the resonant input voltage falls below the instantaneous resonant input voltage.

The dead-time controller may be configured to limit the instantaneous resonant input voltage between a lower threshold voltage and an upper threshold voltage before detecting the local maximum and/or detecting the local minimum. The lower threshold voltage may for example lie between 0.05 and 0.2 times the positive DC supply voltage and the upper threshold voltage may lie between 0.75 and 0.95 times the positive DC supply voltage if the negative DC supply voltage is ground or zero volt.

The dead-time controller may comprise a first digital OR circuit configured to logically OR the first comparator output signal and the first control signal; and
a second digital OR circuit configured to logically OR the second comparator output signal and the second control signal.

As discussed above, the driver circuit and the resonant network are preferably configured for ZVS operation or ZCS operation at the switching frequency of the resonant power converter to charge and discharge the resonant input voltage during the dead-time periods with minimal power consumption.

As discussed previously, the resonant network may comprise a piezoelectric transformer wherein the primary or input section of the piezoelectric transformer is coupled to the resonant input voltage to supply a transformer input voltage. The secondary section of the piezoelectric transformer may generate the resonant output voltage.

A second aspect of the invention relates to a method of adaptively controlling a dead-time interval of a driver circuit of a resonant power converter. The method may comprise steps of:
generating first and second non-overlapping driver control signals for the driver circuit in accordance with a switching frequency signal of the resonant power converter, wherein the driver circuit is coupled between positive and negative DC supply voltages for supply of power,
applying the first and second non-overlapping driver control signals to the driver circuit to generate a driver output signal alternating between the positive DC supply voltage and negative DC supply voltage separated by intervening dead-time periods or intervals,
applying the driver output voltage to an input terminal of the resonant network to generate a resonant input voltage,
generating a resonant output voltage in response to the resonant input voltage at an output side or terminal of the resonant network ,
detecting a feature of the resonant input voltage,

adjusting a duration of the dead-time interval or period of the driver circuit based on the detected feature of the resonant input voltage.

The method may comprise detecting the instantaneous resonant input voltage in each switching cycle of the switching frequency of the resonant power converter and adjusting the dead-time period adjusted accordingly in response. Other embodiments, may be adjusting the dead-time periods less frequently for example during every second, third or fourth switching cycle of the resonant input voltage. The resonant power converter may comprise a rectification circuit coupled to the resonant output voltage of the resonant network for example an output signal of the secondary side of a transformer such as the piezoelectric transformer. The rectification circuit may comprise a half-wave rectifier or a full-wave rectifier.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described in more detail in connection with the appended drawings, in which:

FIG. 1 shows a simplified schematic block diagram of a prior art piezoelectric power converter,

FIGS. 1A, 1B and 1C show respective plots of equivalent circuits and resonant current flow of the piezoelectric transformer of the piezoelectric power converter during eight separate time sub-intervals of a switching cycle,

FIG. 2A) shows corresponding waveforms of transformer input voltage and resonant current during one switching cycle of the prior art piezoelectric power converter in steady state operation where ZVS is achieved,

FIG. 2B) shows corresponding waveforms of transformer input voltage and resonant current during one switching cycle of the prior art piezoelectric power converter in steady state operation where ZVS is achieved,

FIG. 3A) shows a first example of corresponding waveforms of the transformer input voltage and resonant current during one switching cycle of the prior art piezoelectric power converter during a start-up phase or period of the converter,

FIG. 3B) shows a second example of corresponding waveforms of the transformer

input voltage and resonant current during one switching cycle of the prior art piezoelectric power converter in steady state operation,

FIG. 4A) shows corresponding waveforms of the resonant input voltage and resonant current during one switching cycle of a resonant power converter, based on a piezoelectric transformer, in accordance with a first embodiment of the invention in steady state operation where the dead-time period is optimum and ZVS is achieved,

FIG. 4B) shows corresponding waveforms of the resonant input voltage and resonant current during one switching cycle of the piezoelectric power converter in accordance with the first embodiment during a start-up phase or period where the dead-time period is optimum,

FIG. 5 is a simplified schematic circuit diagram of the resonant power converter in accordance with the first embodiment of the invention,

FIG. 5A is a simplified schematic circuit diagram of a resonant power converter based on a LCC power converter in accordance with a second embodiment of the invention,

FIG. 6 is a schematic block diagram of a preferred embodiment of the dead-time controller of the first and second embodiments of the resonant power converter; and

FIG. 7 shows experimentally measured normalized voltage and current waveforms of the transformer input voltage and resonant current of the piezoelectric power converter captured through several switching cycles of the start-up phase and corresponding waveforms of a prior art piezoelectric power converter.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The below-appended description of preferred embodiments of the piezoelectric power converters uses the following:

NOMENCLATURE:

V_F: Transformer input voltage or switching voltage.

i_{res}: Resonant current of piezoelectric transformer.

I_{pk} : Peak value of the resonant current of the piezoelectric transformer.

ω : Switching angular frequency.

Cd1: Input electrode capacitance of the piezoelectric transformer.

Cd2: Output electrode capacitance of the piezoelectric transformer.

R: Dielectric losses inside the piezoelectric transformer.

C: Resonant capacitance of the piezoelectric transformer.

L: Internal inductance of the piezoelectric transformer.

C_{oss}: Output capacitance of MOSFETs of a driver circuit.

C_{in}: Equivalent input capacitance of the piezoelectric transformer attached to a driver circuit.

DT: Dead time.

ODT: Optimum dead time.

FIG. 1 shows a simplified schematic block diagram of a prior art resonant power converter 100 based on a piezoelectric transformer 104. The piezoelectric transformer, PT, 104 is represented by a simplified equivalent electric circuit diagram inside box 104. A lower waveform plot 101 of FIG. 1 shows various voltage and current waveforms of the prior art piezoelectric power converter 100 during operation at a certain switching or excitation frequency as discussed in further detail below. The piezoelectric power converter 100 additionally comprises an input driver circuit 103 electrically coupled to an input electrode of the piezoelectric transformer 104 for receipt of transformer input voltage V_F. Hence, the transformer input signal applies an ac input drive signal to the input or primary section of the piezoelectric transformer 104. A driver control circuit (not shown) may be generating appropriately timed gate control signals for NMOS transistors S_1 and S_2 of the input driver 103. A second input electrode of the piezoelectric transformer 104 may be connected to a negative DC supply rail such as ground, GND, as illustrated. An electrical load R_L may be coupled between a pair of output electrodes of the piezoelectric transformer 104. The pair of pair of output electrodes is electrically coupled to a secondary or output section of the piezoelectric transformer 104 as indicated by the 1:N transformer symbol.

In piezoelectric power converters switches are normally semiconductor devices such as MOSFETs with a build-in delay time. This delay time applies to a gate drive signal to start up a switching of the state of the semiconductor switch. Typically, the turn on and turn off delay time of the semiconductor switch differs. Therefore, an amount of delay is given to the gate drive signal to prevent simultaneous conducting states on of the semiconductor switches. Therefore, a dead time period or interval is usually defined as a time interval during a switching transition where both semiconductor switches, e.g. MOSFETs, are in non-conducting states, i.e. turned off. A driv-

er circuit with a half-bridge topology, coupled to an input electrode of the piezoelectric transformer, should preferably have a dead-time period arranged in-between the conducting state periods of the semiconductor switches in order to avoid cross-conduction or shoot through between the semiconductor switches. In piezoelectric power converters, the semiconductor switches of the driver circuit need to supply reactive energy to an input capacitor or capacitance associated with the primary section of the piezoelectric transformer. However, the dead-time period provides appropriate time for charging and discharging this input capacitance of the primary section of the piezoelectric transformer. In contrast only MOSFET's output capacitances need to be charged by resonant current of LCC resonant power converters. These MOSFET's output capacitances are typically around hundreds of pF.

In piezoelectric power converters, the output capacitances of the semiconductor switches and the input capacitance associated with the primary section of the piezoelectric transformer must be charged by resonant current to raise the resonant input voltage at input electrode from the negative DC supply voltage or rail, e.g. ground 0 (V), to the positive DC supply voltage or rail as previously discussed. Since the input capacitance associated with the primary section of the piezoelectric transformer is normally in the range of nF it requires longer time for the resonant current to provide enough charge to the capacitances. Hence, the dead-time of the input driver of a piezoelectric power converter is normally longer or larger than the dead-time of the input driver of a LCC resonant converter. It is often advantageous to keep the dead-time of the input driver of a piezoelectric power converter as short as possible in order to increase power conversion efficiency. Furthermore, this feature will prolong injection of energy to the piezoelectric transformer during turn on time of a high side switch pulling the input the output of the driver circuit towards the positive DC supply voltage. The behaviour of input inductor less piezoelectric power converters where ZVS operation of the input driver circuit is achieved is analysed in the following with reference to the different operating modes illustrated on the plots of FIGS. 1A, 1B and 1C. The present analysis is generally carried out for 8 different operating modes which are divided into 4 intervals. Each of these 4 intervals comprises 2 subintervals as discussed below. Therefore, voltage waveforms of the transformer input voltage V_F through a switching cycle of the input voltage are shown as $t_0 - t_{12}$ with respect to V_F. FIG. 2 shows both the transformer input voltage V_F and corresponding resonant

current I_{res} waveforms during one switching cycle in steady state of the piezoelectric power converters where ZVS operation is achieved. The plots a-h of FIGS. 1A), 1B) and 1C) show eight different operating modes. The below-appended analysis is based on the following three assumptions:

1) The converter's input capacitor is considered as summation of the input capacitance C_{d1} of the piezoelectric transformer 104 and the sum of output capacitances of the first and second semiconductor switches S_1 and S_2, typically MOSFETs,

$$C_{in} = 2\,C_{oss}+C_{d1} \qquad (1)$$

2) Negligible parasitic components;

3) Fundamental resonating of the piezoelectric transformer due to its high quality factor.

Therefore, Mason's lumped circuit is used to demonstrate operation of the piezoelectric power converter in terms of resonant current and switching voltages of the semiconductor switches S_1 and S_2 of the input driver 103. Resonant current is also illustrated to allow detailed investigation of the operating modes. Output capacitors of S_1 and S_2 and C_{d1} are considered to be the input capacitance of the input section of piezoelectric transformer 104 since parasitic capacitances of a MOSFET based semiconductor switch is typically much lower than C_{d1} or in the other hand they would be charged and discharged together in the dead-time period. Furthermore, the dead-time period is studied in detail below.

1) S_2 is in a conducting switch state or ON while S_1 is in a non-conducting switch state or OFF state: Time interval $t_{12} – t_2$. The input capacitance of the piezoelectric transformer 104 is fully discharged and essentially short circuited through the relatively small on-resistance of semiconductor switch S_2 which is a low-side switch of the input driver. At t_{12} S_2 is turned on and resonant current I_{res} freewheels through S_2 and changes direction at some point in time which is labelled as t_{1l}. There is a minor voltage difference across S_2 while it is conducting. At time instant t_{1l} the resonant current has crossed zero and changes direction from forward to reverse and the

operation of the piezoelectric power converter is illustrated in two subintervals by plots a and b of FIG. 1A. Plot a and plot b show an equivalent circuit and a resonant current flow during each of these time intervals. The below listed set of equations (2) formulates the resonant current and the switching voltage at this interval.

$$\begin{cases} V_F(t) = 0 \\ i_{res}(t) = I_{pk}\, sin(\omega t - \phi_I) \end{cases} \quad (2)$$

2) Both S_2 and S_1 are in a non- conducting switch state or OFF: Time interval $t_2 - t_5$. During this time interval both semiconductor switches are OFF and the resonant current keeps its direction in the reverse orientation going through C_{d1} to a voltage slightly above the positive DC supply voltage V_{DC} until a high-side body diode, i.e. the body diode 113a of MOSFET switch S_1, clamps the transformer input voltage V_F at $V_{DC.}$ Plot c of FIG. 1A shows the equivalent circuit and current flow in this time interval and the set of equations (3) below describes the voltage and current waveforms.

$$\begin{cases} V_F(t) = \frac{I_{pk}}{C_{in}} (cos(\omega t - \phi_I) - cos(\omega t_2 - \phi_I)) + 0 \\ i_{res}(t) = I_{pk}\, sin(\omega t - \phi_I) \end{cases} \quad (3)$$

During time interval $t_5 - t6$, the high-side body diode 113a of MOSFET switch S_1 starts to conduct reverse resonant current. Therefore, the transformer input voltage V_F is clipped to the sum of diode voltage drop across the body diode and V_{DC}. This time interval is not requisite because C_{d1} is already charged sufficiently to produce ZVS or soft switching. Plot d of FIG. 1B shows the equivalent circuit and current flow in this time interval and the set of equations (4) below describes the voltage and current waveforms.

$$\begin{cases} V_F(t) = V_{DC} + V_d \\ i_{res}(t) = I_{pk}\, sin(\omega t - \phi_I) \end{cases} \quad (4)$$

3) S_1 is in a conducting switch state or ON while S_2 is in a non-conducting switch state or OFF: Time interval $t_6 - t_8$. The high side MOSFET S_1 is conducting and the resonant current I_{res} freewheels through S_1 to be provided to the piezoelectric transformer. There is in practice a minor voltage difference across the finite on-resistance of S_1 while conducing. At t_{2l} the resonant current I_{res} has crossed zero or ground and changes direction from reverse to forward. The operation of the piezoelectric power converter is therefore illustrated in two subintervals by plots e and f of FIG. 1B. The plots e and f show an equivalent circuit and current flow during each of these time intervals. The below listed set of equations (5) formulates the resonant current and the switching voltage V_F during this time interval.

$$\begin{cases} V_F(t) = V_{DC} \\ i_{res}(t) = I_{pk}\, sin(\omega t - \phi_I) \end{cases} \quad (5)$$

4) Both S_2 and S_1 are in a non- conducting switch state or OFF: Time interval $t_8 - t_{12}$. At time instant t_8 the high-side switch S_1 is turned off. During this interval both S_2 and S_1 are in OFF states and the resonant current I_{res} keeps its direction in the forward orientation by being fed through the input capacitance C_{d1}. The input capacitance C_{d1} is discharged and the voltage across C_{d1} drops to a level slightly below ground until a low side body diode 113b of S_2 clamps at time instant t_{1l}. Plot g of FIG. 1C shows the equivalent circuit and current flow in this time interval and the set of equations (6) below describes the voltage and current waveforms of I_{res} and V_F.

$$\begin{cases} V_F(t) = \frac{I_{pk}}{C_{in}} (cos(\omega t - \phi_I) - cos(\omega t_8 - \phi_I)) + V_{DC} \\ i_{res}(t) = I_{pk}\, sin(\omega t - \phi_I) \end{cases} \quad (6)$$

Time interval $t_{1l} – t_{12}$: At t_{1l} the low side body diode of S_2 starts to conduct forward the resonant current. Therefore, the transformer input voltage V_F is clipped at a level of one diode voltage drop below ground. This time interval is not requisite because C_{d1} is already discharged completely to produce ZVS or soft switching. Plot h of FIG. 1C shows the equivalent circuit and current flow in this time interval and the set of equations (7) below describes the resonant current and the switching voltage V_F during this time interval.

$$\begin{cases} V_F(t) = -V_d \\ i_{res}(t) = I_{pk}\, sin(\omega t - \phi_l) \end{cases} \qquad (7)$$

As previously mentioned it is important to have a sufficient duration or length of the intervening dead-times periods between the alternatingly conducting switch states of the first and second semiconductor switches S_1 and S_2. The duration of each of these dead time periods have often been shorter or longer than required to provide optimal ZVS operation for the reasons discussed above. This situation causes so-called hard switching of the first and and/or second semiconductor switches S_1 and S_2 and leads to a marked increase of the power consumption of the driver circuit. FIGS. 2A) and 2B) show these situations in the steady state operation of the prior rat piezoelectric power converter 100 depicted schematically on FIG. 1.

In contrast, the piezoelectric power converter 500 in accordance with the first embodiment of the present invention provides soft-switching of the first and and/or second semiconductor switches S_1 and S_2 of the driver circuit 503 by making an appropriate adaptation of the dead-time period of the driver circuit. In this manner, the dead-time may be adaptively adjusted to charge and discharge the input capacitance C_{d1} of the piezoelectric transformer 504 to the positive DC supply voltage V_{DC} and the negative DC supply voltage - for example ground or 0 V. FIG. 5 shows one embodiment of a piezoelectric power converter 500 in accordance with the present invention where a dead-time controller is configured to adaptively adjust a duration of the dead-time periods based on the transformer input voltage V_F as discussed in

further detail below. In addition, FIG. 5A shows a magnetics based LCC topology of resonant power converter 500a in accordance with a second embodiment of the present invention where a dead-time controller is configured to adaptively adjust durations of the dead-time periods based on the resonant input voltage V_F as discussed in further detail below.

FIG. 2A) shows the situation where the dead-time period is shorter than optimum because the first and second semiconductor switches S_1 and S_2 are turned ON too early before the input capacitance C_{d1} is fully charged or discharged, respectively, to the DC supply voltage in question. This situation leads to hard switching of the driver circuit as shown by the respective waveforms 222a, 222b of the instantaneous transformer input voltage V_F and the corresponding resonant current I_{res}.

FIG. 2B) shows the situation where the dead-time period is longer than optimal because the first and second semiconductor switches S_1 and S_2 are turned ON too late. This situation also leads to hard switching of the driver circuit as shown by the respective waveforms 223a, 223b of the instantaneous transformer input voltage V_F and the corresponding resonant current I_{res}. In this case when the resonant current changes direction, the body diodes of the first and second semiconductor switches S_1 and S_2 are not conducting. This causes the input capacitance C_{d1} to discharge at time instant t_{2l} or being charged at t_{1l} before the semiconductor switches are turned on.

In prior art resonant power converters, such as piezoelectric power converters, the dead-time period has been a fixed time or value for the purpose of ensuring that ZVS operation is achieved in the steady state operation of the resonant power converter. This fixed dead-time period is normally longer than the optimal dead-time period discussed above. Another disadvantage of this fixed dead-time period is the build-up of resonant current is delayed during initialization or start-up of the prior art resonant power converter and it takes longer time for the converter to reach steady state operation. While this prolonged start-up time may seem rather insignificant in general, it becomes an important source of excess power consumption in resonant power converters that are turned on and turned off very frequently. This pattern of frequent turn off and turn off of the resonant power converter is for example utilized

in so-called burst-mode control or quantum-mode control of the output voltage of the resonant power converter.

The present resonant power converter embodiments eliminate the cases shown in FIGS. 2A) and 2B) with too short or too long dead-time periods, compared to the optimal dead-time period. The piezoelectric power converter embodiment 500 depicted on FIG. 5 comprises the previously discussed dead-time controller OTD 514 which may dynamically detect and set an optimized dead time during every switching cycle of the transformer input voltage V_F. The operation of dead-time controller 514 optimizes, for example during each switching cycle, the time instants where the semiconductor switches S_2 and S_1 are switched from OFF to ON, i.e. turned on, to be placed substantially where the instantaneous transformer input voltage V_F reaches either the positive DC supply voltage or reaches the negative DC supply voltage during steady-state operation of the power converter. Furthermore, the dead-time controller 514 may also be configured to optimize the switching instants of the semiconductor switches S_2 and S_1 during the previously discussed initialization or start-up phase of the power converter. In the latter case, the operation of dead-time controller 514 optimizes, during each switching cycle, the time instants where the semiconductor switches S_2 and S_1 are switched from OFF to ON, i.e. turned on, to be placed substantially where the instantaneous transformer input voltage V_F reaches either a minima level or a maxima level. This may be accomplished by detecting or monitoring the waveform shape of the instantaneous transformer input voltage V_F as discussed in additional detail below. FIG. 4A) shows exemplary waveforms of the transformer input voltage V_F and resonant current I_{res} of the piezoelectric power converter 500 during steady-state operation of the power converter 500. The two consecutive dead-time periods of the depicted single switching cycle of the transformer input voltage V_F are indicated by legend ODT. As shown by the waveform segment 422a, the transformer input voltage V_F increases monotonically from the negative DC supply voltage for ground (0 V) to the positive DC supply voltage $V_{DC.}$ This increase of voltage is caused by the conducting state of the first semiconductor switch S_1 (and hence non-conducting state of S_2) which is pulling the transformer input voltage V_F towards V_{DC} via the small on-resistance of switch S_1. Likewise, the monotonically decreasing waveform segment 422b of the transformer input voltage V_F from the positive DC supply voltage V_{DC} to the negative DC supply voltage (0 V) is

caused by the small on-resistance of switch S_2 which is pulling the transformer input voltage V_F towards 0 V or ground.

As shown in FIG. 1B), there are two dead time period periods or intervals in each switching cycle and these dead-time periods correspond to the time intervals $t_2 – t_6$ and $t_8 – t_{12}$ described above. Two time subintervals $t_2 – t_4$ and $t_8 – t_{10}$ are necessary to reach voltage across C_{d1} to the positive and negative DC supply voltage for obtaining ZVS operation of the driver circuit. In effect, the optimum dead time period is may reasonably be defined as a minimum time required for the resonant input voltage V_F to travel from one of the positive and negative DC supply voltages or rails to the other. Therefore, by detecting the time instants or points where the resonant input voltage V_F reaches either the positive or the negative DC supply voltage the time intervals $t_4 – t_6$ and $t_{10} – t_{12}$ can be reduced to a minimum possible time. This is utilized in one embodiment of invention. On the other hand, optimizing the respective time intervals $t_2 – t_4$ and $t_8 – t_{10}$ is achieved by detection of time instant t_4 and detection of of time instant t_{10} as shown in Fig. 4A). The latter detection allows the dead-time controller 514 to turn on the first and second semiconductor switches S_1 and S_2 at these time instants or points, respectively. This results in the setting of the optimum dead time period during each switching cycle of the resonant input voltage V_F. This feature results in fast and power efficient start-up of the resonant current I_{res} by maximizing respective conducting state time periods of the first and second semiconductor switches S_1 and S_2 in order to feed energy into the resonant tank, e.g. including a primary side of the piezoelectric transformer, and build up resonant current.

The skilled person will appreciate that the detection of the time instants or points where the instantaneous transformer input voltage V_F reaches either the positive or negative DC supply voltage under steady state operation may be accomplished by different types of analog, digital or mixed-signal circuitry as discussed below in further detail. The previously discussed start-up phase or time period of the power converter designates the time period from power-on of the power converter to the time instant where the resonant current in the piezoelectric transformer reaches the maximum amplitude in the operating point of the power converter. During this start-up phase, the resonant current is growing continuously, but it does not reach the

highest possible amplitude. Therefore, the input capacitance C_{d1} will not be charged all the way up to the level of the positive DC supply voltage or discharged all the way down to the level of the negative DC supply voltage.

FIGS. 3A) and 3B) show exemplary voltage and current waveforms of V_F and I_{res} during the start-up phase or period of the prior art power converter 100.

Accordingly, two different situations may be encountered during the dead time period DT in the start-up period: In a first situation, the instantaneous transformer input voltage V_F may pass through local maximum/minimum before the semiconductor switches are turned on. FIG 3B) shows waveforms 323a, 323b of V_F and I_{res} for this situation. The presence of the maximum/minimum or extrema in V_F at time instant t_{2l} of the waveform 323a is caused by a change of direction of the resonant current I_{res} during the first dead time period DT as indicated by the zero-crossing of I_{res} at the time instant t_{2l}. Therefore, the resonant current I_{res} changes from charging to discharging the input capacitance C_{d1}. In the second situation, the transformer input voltage V_F is still increasing or decreasing until the first or second semiconductor switch S_1 or S_2 is turned on. This means that the transformer input voltage V_F will not pass through any local extrema. In this situation, the amplitude of the resonant current I_{res} is too small to fully charge the input capacitance C_{d1}. This second situation is illustrated by the waveforms 322a, 322b of V_F and I_{res} of FIG. 3A). The resonant current I_{res} is changing direction during a switching cycle. The amplitude of the resonant current leads to the difference between the first and second situations which may be encountered during the start-up period. The resonant current I_{res} is build up after power-on of the power converter and gradually increases in amplitude until the resonant current I_{res} reaches a steady state amplitude. During steady state operation, the amplitude of the resonant current I_{res} remains essentially constant provided the input voltage, temperature and load of the power converter also remain essentially constant. At the beginning of the start-up time period, the amplitude of the resonant current I_{res} is so small that I_{res} is unable to fully charge the the input capacitance C_{d1} during the dead time period to the positive DC supply voltage. This deficiency applies to both of the charging processes illustrated by FIG. 3A) and FIG. 3B). The optimal charging process may reasonably be considered reached by adapting the charging process of the input capacitance C_{d1} as illustrated by FIG.

4B). In the latter charging process the resonant current I_{res} is near its peak amplitude at time instant t_2 when dead time period starts.

It can be shown that the total amount of energy provided to the input capacitance C_{d1} in the dead time period, defined as $\Delta t = t_6 - t_2$, is:

$$\Delta E = \frac{I_{pk}^2}{4C_{in}}\left(1 - \frac{1}{2\omega\Delta t}sin(2\omega\Delta t)\right) \qquad (15)$$

Therefore, it is important to turn on the first semiconductor switch S_1 or the second semiconductor switch S_2 at the zero crossing of the resonant current I_{res} depicted on FIG. 4B). Consequently, to optimize the dead time period either during the start-up phase of the power converter or during the steady state operation thereof, one embodiment of the dead-time controller 514 may be configured to switch the first or second semiconductor switch to its conducting state either when the transformer input voltage V_F reaches one of the positive and negative DC supply voltages or when the resonant current I_{res} crosses zero which ever condition occurs first. If neither of these conditions are detected the dead-time controller 514 may apply a fixed dead time period to facilitate build-up of the resonant current I_{res}. The skilled person will understand that there is no direct access to detect or measure the resonant current I_{res} inside the piezoelectric transformer 513. Therefore, the transformer input voltage V_F may conveniently be used by the dead-time controller 514 as a reference for detecting the dead time period in the piezoelectric power converter 500.

The LCC resonant power converter 500a of FIG. 5A in accordance with the second embodiment of the present invention likewise eliminates cases corresponding to those shown in FIGS. 2A) and 2B) with too short or too long dead-time periods of the resonant input voltage, compared to the optimal dead-time period. The LCC power converter 500a comprises a resonant network or circuit comprising first capacitor C and a first inductor L connected in series to the resonant input voltage V_F applied at the input terminal 507a of the resonant network. The resonant network additionally comprises a second capacitor C_p coupled in parallel across a primary side of a magnetic transformer with conversion ratio 1:N. Hence, the resonant voltage across the primary side of the magnetic transformer may be an output voltage

of the resonant network. A secondary side of the magnetic transformer is coupled to a load R_L. Other embodiments of the resonant power converter 500a may comprise a rectification circuit coupled to the secondary side of the magnetic transformer to generate a DC output voltage of the LCC power converter 500a. A resonant current I_{res} is flowing through the first inductor L of the resonant network to alternatingly charge and discharge the resonant input voltage V_F during successive dead-time periods of the half-bridge driver 503a. The LCC power converter 500a comprises a dead-time controller OTD 514a which may be configured to dynamically detect and set an optimized dead time period during every switching cycle of the resonant input voltage V_F. The operation of the dead-time controller 514a may optimize, during each switching cycle or at least a majority of switching cycles, the time instants where the semiconductor switches S_2 and S_1 of the driver 501a are switched from OFF to ON to be placed substantially where the instantaneous resonant input voltage V_F reaches either the positive DC supply voltage or reaches the negative DC supply voltage during steady-state operation of the LCC power converter 500a. This may be accomplished by adjusting the phase or timing of the first and second driver control signals HS_G, LS_G as discussed in detail below with reference to FIG. 6. Furthermore, the dead-time controller 514a may also be configured to optimize the switching instants of the semiconductor switches S_2 and S_1 of the driver circuit 503a during an initialization or start-up phase of the LCC power converter 500a. In the latter case, the operation of dead-time controller 514 optimizes, during each switching cycle, the time instants where the semiconductor switches S_2 and S_1 are switched from OFF to ON, i.e. turned on, to be placed substantially where the instantaneous resonant input voltage V_F reaches either a minima level or a maxima level during a dead-time period. This may be accomplished by detecting or monitoring the waveform shape of the instantaneous resonant input voltage V_F in a manner correspond to the one discussed in additional detail below with reference to FIG. 6. The operation and characteristics of the gate driver 501a and driver circuit 503a are also discussed in additional detail below with reference to the corresponding gate driver 501 and driver circuit 503 of the first embodiment of the resonant power converter 500.

FIG. 6 is a schematic block diagram of a preferred embodiment of the dead-time controller 514 of the piezoelectric power converter 500. The dead-time controller

514 comprises *inter alia* a steady-state controller 624 and a start-up controller 634 and a control circuit 644 (OTD C). The steady-state controller 624 is adapted to generate appropriately timed first and second driver control signals HS_G, LS_G for the for the half-bridge driver 503, delivered through the optional gate drive 501, and during steady-state operation of the power converter 500 and the corresponding first and second driver control signals HS_G, LS_G for the half-bridge driver 503a during steady-state operation of the LCC resonant power converter 500a. The start-up controller 634 is adapted to generate appropriately timed first and second driver control signals HS_G, LS_G for the half-bridge drivers 503, 503a during the initialization time or start-up time of the power converters 500, 500a. Hence, the first driver control signal HS_G switches the first or high side semiconductor switch S_1 between its conducting state and non-conducting state and the second driver control signal LS_G switches the second semiconductor switch S_2 between its conducting state and non-conducting state. Body diodes D_1 and D_2 are associated with the semiconductor switches S_1 and S_2, respectively, and may have the same function as the previously discussed body diodes 113a, 113b. Each of the first and second semiconductor switches S_1 and S_2 preferably comprises a MOSFET. The output of the driver circuit 503 supplies the transformer input voltage V_F since the output node of the driver circuit 503, i.e. the mid-point node between respective drain terminals of the MOSFET semiconductor switches S_1 and S_2, is coupled directly to a first input electrode 507a of an input section or primary side of the piezoelectric transformer 513. A second input electrode 507b of the primary side of the piezoelectric transformer 513 may be coupled to GND. The dead-time controller 514 is electrically connected to the transformer input voltage V_F and to the second input electrode 507b. The piezoelectric transformer 513 may further comprise a pair of output electrodes 508a, 508b electrically coupled to a secondary or output section of the piezoelectric transformer 513 and supply a transformer output voltage to an input of a rectification circuit 508. The rectification circuit 508 may comprise a half wave or full wave rectifier, and possibly output capacitor(s), to provide a smoothed DC voltage at an output node or terminal V_{OUT} of the piezoelectric power converter 500.

The steady-state controller 624 comprises a first comparator 625 configured to compare the instantaneous level or value of the transformer input voltage V_F to the positive DC supply voltage V_{DC}, fed through terminal or line 622, and supply a first

comparator output signal Z_{HS}. The first comparator output signal Z_{HS} is utilized for adjusting the phase of the first driver control signal HS_G (please refer to FIG. 5) via the logic control circuit 644. The first driver control signal HS_G is applied to a control or gate terminal of the first semiconductor switch S_1 of the driver circuits 503, 503a. The steady-state controller 624 additionally comprises a second comparator 627 configured to compare the instantaneous level or amplitude of the transformer input voltage V_F to the negative DC supply voltage, which is ground or 0 V in the present embodiment, fed through terminal or line S, 623, and supply a second comparator output signal Z_{LS}. The second comparator output signal Z_{LS} is utilized for adjusting a phase of a second driver control LS_G (please refer to FIG. 5) via the logic control circuit 644. The second driver control signal LS_G is applied to the control or gate terminal of the second semiconductor switch S_2 of the half-bridge driver 503, optionally via the gate drive 501.

The start-up controller 634 is configured to detect a waveform shape of the transformer input voltage V_F and generate a first control signal Z_{MH} for adjusting the timing or phase of the first driver control signal HS_G via the logic control circuit 644 in accordance with the waveform shape of the transformer input voltage V_F. The start-up controller 634 is preferably also configured to detect a waveform shape of the transformer input voltage V_F and generate a second control signal Z_{ML} for adjusting the timing or phase of the second driver control signal LS_G via the logic control circuit 644 in accordance with the waveform shape of the transformer input voltage V_F. During the initialization period or start-up phase or period of the piezoelectric power converter 500, the instantaneous transformer input voltage V_F is applied at line or terminal 620, signal S, and compared with a delayed replica of the transformer input voltage S_d. The delayed replica of the transformer input voltage S_d is applied to a negative input of a third comparator 639 of the circuit 514. A local local maximum of the waveform of the instantaneous transformer input voltage is detected when S_d > signal S. Hence, the local maximum of the waveform of the instantaneous transformer input voltage during a dead-time period with increasing resonant input voltage is detected in response to, or when, the voltage of the delayed replica S_d exceeds signal S. Likewise, a local minimum of the waveform of V_F during a dead-time period with decreasing or falling resonant input voltage is detected when signal S < signal S_d (the delayed replica of the transformer input voltage).

The start-up controller 634 may furthermore limit the instantaneous transformer input voltage V_F between a predefined lower threshold voltage and a predefined upper threshold voltage before detecting the above-discussed local local maximum and minimum of the waveform of the instantaneous transformer input voltage. In the present embodiment, the start-up controller 634 is configured to set an intermediate or middle voltage range (M) between the predefined lower threshold voltage V_{Low} and the predefined upper threshold voltage V_{Hi} via the corresponding reference voltages applied through input lines or terminals 616 and 618 of the start-up controller 634. The predefined lower threshold voltage V_{Low} may for example be around 10 % of the positive DC supply voltage V_{DC} such as between 0.05 and 0.2 times V_{DC} when the negative DC supply voltage is ground as in the present embodiment. The predefined upper threshold voltage V_{Hi} may for example be around 90 % of the positive DC supply voltage V_{DC} such as between 0.75 and 0.95 times V_{DC}. These value ranges for the predefined lower and upper threshold voltages will provide a suitable noise margin for local extrema detection and prevent undesired triggering by noise impulses of the transformer input voltage. A fourth comparator 636 indicates whether the instantaneous transformer input voltage on line S is above the predefined lower threshold voltage V_{Low}. A fifth comparator 638 indicates whether the instantaneous transformer input voltage on line S is below the predefined upper threshold voltage V_{Hi}. The third comparator 639 may comprise a high precision dual/differential output comparator. As mentioned above, the output signals $HS_{G,}$ LS_G of the ODT C block are controlled by the control circuit or block 644 in accordance with logic states of the input signals Z_{MH}, Z_{ML}, Z_{HS} and Z_{LS}. The first semiconductor switch S_1 is switched ON in response to either Z_{HS} or Z_{HM} is asserted such that HS_G is logically “1”. The second semiconductor switch S_2 is turned/switched ON in response to either Z_{LS} or Z_{ML} is asserted or digitally “1” such that LS_G is logically “1”. A reset control signal "R" through line 645 of the control circuit or block 644 is configured to selectively switching off the first and second semiconductor switches S_1 and S_2 after the allocated ON time period of the semiconductor switch in question. Finally, an optional enable signal "En" and function received through line 647 may enable/disable the operation of the dead-time controllers 514, 514a in the resonant power converters 500, 500a. The skilled person will understand that the respective voltage levels of references voltages such as V_{Hi}, V_{DC} and V_{Low} utilized in the dead-time controller 514 may be scaled to a voltage level of the comparators 625, 627, 639, 636, 638. The particular

Boolean functions implemented in the dead-time controller 514 for the outputs of the steady-state controller 624 and the start-up controller 634 are:

$$\begin{cases} Z_{ML} = (S < V_{Hi}) \cdot (S > S_d) \\ Z_{MH} = (S > V_{Low}) \cdot (S < S_d) \\ Z_{HS} = (S > V_{DC}) \\ Z_{LS} = (S < 0) \end{cases} \quad (16)$$

$$\begin{cases} HS_G = (Z_{HS} + Z_{MH}) \cdot En \cdot \overline{R} \\ LS_G = (Z_{LS} + Z_{ML}) \cdot En \cdot \overline{R} \end{cases} \quad (17)$$

The steady-state controller 624 comprises the first comparator 625 which is configured to comparing the transformer input voltage V_F to the positive DC supply voltage V_{DC} via the positive and negative inputs of the first comparator 625. The positive input of the first comparator 625 receives the transformer input voltage V_F via line or terminal 620. The second comparator 627 is configured to comparing the transformer input voltage V_F to the negative DC supply voltage, i.e. 0 V via the positive and negative inputs of the second comparator 627.

Overall, the first and second semiconductor switches S_1 and S_2 are turned on, i.e. switched to the conducting state, by a rising edge of Z_{HS} and Z_{LS}, respectively, in the steady state operation of the resonant power converters 500, 500a. Likewise, the first and second semiconductor switches S_1 and S_1 are turned off, i.e. switched to the non-conducting state, by a falling edge of Z_{HS} and Z_{LS}, respectively, in the steady state. The same control scheme applies during the start-up or initialization period of the resonant power converters 500, 500a and the logic control block 644 determines whether first and second driver control signal $HS_{G,}$ LS_G for the first and second sem-

iconductor switches S_1 and S_2 are derived from the outputs of the steady-state controller 624 or the outputs of the start-up controller 634. Hence, each of the driver circuits 501, 503, 501a, 503a is configured to alternatingly pulling the resonant or transformer input voltage V_F towards the positive and negative DC supply voltages or rails via the first and second semiconductor switches S_1 and S_2, respectively, separated by intervening dead-time periods during each switching cycle in accordance the first and second driver control signals HS_G, LS_G.

The lower plot 1020 of FIG. 7 shows experimentally measured normalized voltage and current waveforms of the transformer input voltage V_F and resonant current I_{res} captured through several switching cycles of a start-up phase or state of the piezoelectric power converter 500 in comparison with the corresponding waveforms on the upper plot 1010 of the exemplary prior art piezoelectric power converter 100 depicted on FIG. 1A. The measurements were performed on a radial mode piezoelectric transformer with the following parameters:

Parameter	Value	Parameter	Value
C_{d1}	3.8 nF	C_{d2}	626 pF
C	565 nF	R	5.6 Ω
L	3.5 mH	N	3.5

Furthermore, the fundamental resonance frequency of the radial mode piezoelectric transformer was 116.3 kHz and the load Z_L was a resistive load corresponding to 300 W of output power.

CLAIMS

1. A resonant power converter comprising:
a first power supply rail for receipt of a positive DC supply voltage and a second power supply rail for receipt of a negative DC supply voltage,
a resonant network comprising an input section and an output section wherein the input section comprises an input terminal for receipt of a resonant input voltage and the output section comprises an output terminal for providing a resonant output voltage in response to the resonant input voltage,
a driver circuit comprising a first semiconductor switch coupled to the positive DC supply voltage and a second semiconductor switch coupled to the negative DC supply voltage and a driver output connected to the input terminal for supply of the resonant input voltage;
wherein the driver circuit is configured for alternatingly pulling the resonant input voltage towards the positive and negative DC supply voltages via the first and second semiconductor switches, respectively, separated by intervening dead-time periods in accordance with one or more driver control signals,
a dead-time controller configured to adaptively adjusting the dead-time periods based on the resonant input voltage.

2. A piezoelectric power converter according to claim 1, wherein the first semiconductor switch comprises a conducting state where the input terminal is connected to the positive DC supply voltage and the second semiconductor switch comprises a conducting state where the input terminal is connected to the negative DC supply voltage; and
where the first semiconductor switches is in a non-conducting state during the dead-time periods and the second semiconductor switch is in a non-conducting state during the dead-time periods.

3. A resonant power converter according to claim 1 or 2, wherein the dead-time controller is configured to adjust a phase of a first driver control signal of the first semiconductor switch and a phase of a second driver control signal of the second semiconductor switch to adaptively adjust the duration of the dead-time pe-

riods.

4. A resonant power converter according to claim 1, wherein the driver circuit comprises a half-bridge wherein the first semiconductor switch and the second semiconductor switch are coupled in series between the positive DC supply voltage and the negative DC supply voltage.

5. A resonant power converter according to claim 3 or 4, wherein the dead-time controller comprises a steady-state controller comprising:
a first comparator configured to compare the instantaneous resonant input voltage to the positive DC supply voltage and supply a first comparator output signal (Z_{HS}) for adjusting the phase of the first driver control signal in accordance with the first comparator output signal,
a second comparator configured to compare the instantaneous resonant input voltage to the negative DC supply voltage and supply a second comparator output signal (Z_{LS}) for adjusting the phase of the second driver control signal in accordance with the second comparator output signal.

6. A resonant power converter according to claim 3 or 4, wherein the dead-time controller comprises a start-up controller configured to detect a waveform shape of the instantaneous resonant input voltage; and
generating a first control signal (Z_{MH}) for adjusting the phase of the first driver control signal in accordance with the waveform shape; and/or
generating a second control signal (Z_{ML}) for adjusting the phase of the second driver control signal in accordance with the waveform shape.

7. A resonant power converter according to claim 6, wherein the dead-time controller is configured to detect the waveform shape of the instantaneous resonant input voltage by comparing the instantaneous resonant instantaneous transformer input voltage with a delayed replica of the resonant input voltage.

8. A resonant power converter according to claim 7, wherein the dead-time controller is configured to:
detect a local maximum of the waveform of the instantaneous resonant input

voltage in response to the delayed replica of the resonant input voltage exceeds the instantaneous resonant input voltage; and/or

detect a local minimum of the waveform of the instantaneous resonant input voltage in response to the delayed replica of the resonant input voltage falls below the instantaneous resonant input voltage.

9. A resonant power converter according to claim 7 or 8, wherein the dead-time controller is configured to limit the instantaneous resonant input voltage between a lower threshold voltage and an upper threshold voltage before detecting the local maximum and/or detecting the local minimum.

10. A resonant power converter according to claim 9, wherein the lower threshold voltage lies between 0.05 and 0.2 times the positive DC supply voltage and the upper threshold voltage lies between 0.75 and 0.95 times the positive DC supply voltage.

11. A resonant power converter according to claim 5 and 6, wherein the dead-time controller comprises a first digital OR circuit configured to logically OR the first comparator output signal and the first control signal; and

a second digital OR circuit configured to logically OR the second comparator output signal and the second control signal.

12. A method of adaptively controlling a dead-time interval of a driver circuit of a resonant power converter, comprising steps of:

generating first and second non-overlapping driver control signals for the driver circuit in accordance with a switching frequency signal of the resonant power converter, wherein the driver circuit is coupled between positive and negative DC supply voltages for supply of power,

applying the first and second non-overlapping driver control signals to the driver circuit to generate a driver output signal alternating between the positive DC supply voltage and negative DC supply voltage separated by intervening dead-time periods or intervals,

applying the driver output voltage to an input terminal of the resonant network to generate a resonant input voltage,

generating a resonant output voltage in response to the resonant input voltage at an output side or terminal of the resonant network ,
detecting a feature of the resonant input voltage,
adjusting a duration of the dead-time interval or period of the driver circuit based on the detected feature of the resonant input voltage.

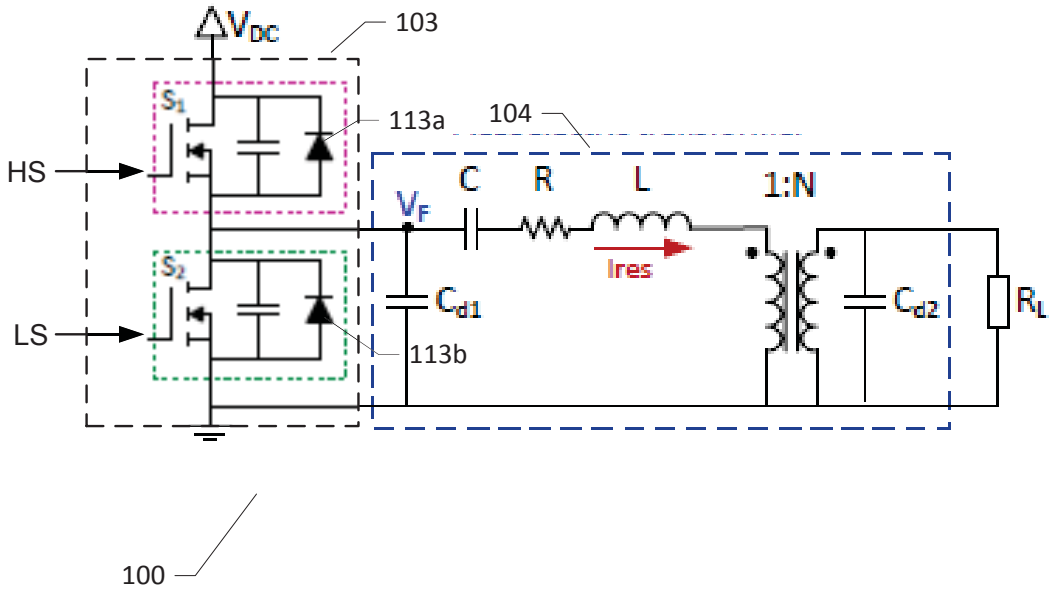
13. A method of adaptively controlling a dead-time period according to claim 12, wherein the instantaneous resonant input voltage is detected in each switching cycle of the switching frequency of the resonant power converter and the dead-time period adjusted accordingly in response.

14. A resonant power converter according to any of the preceding claims, wherein the driver circuit and the resonant network are configured for ZVS operation or ZCS operation at the switching frequency of the resonant power converter.

15. A resonant power converter according to any of the preceding claims, wherein the resonant network comprises a piezoelectric transformer;
wherein a primary section of the piezoelectric transformer is coupled to the resonant input voltage to supply a transformer input voltage and a secondary section of the piezoelectric transformer generates the resonant output voltage.

ABSTRACT

The invention relates in a first aspect to a resonant power converter comprising: a first power supply rail for receipt of a positive DC supply voltage and a second power supply rail for receipt of a negative DC supply voltage. The resonant power converter comprises a resonant network with an input terminal for receipt of a resonant input voltage from a driver circuit. The driver circuit is configured for alternatingly pulling the resonant input voltage towards the positive and negative DC supply voltages via first and second semiconductor switches, respectively, separated by intervening dead-time periods in accordance with one or more driver control signals. A dead-time controller is configured to adaptively adjusting the dead-time periods based on the resonant input voltage.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103
S1
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Cd2
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113b
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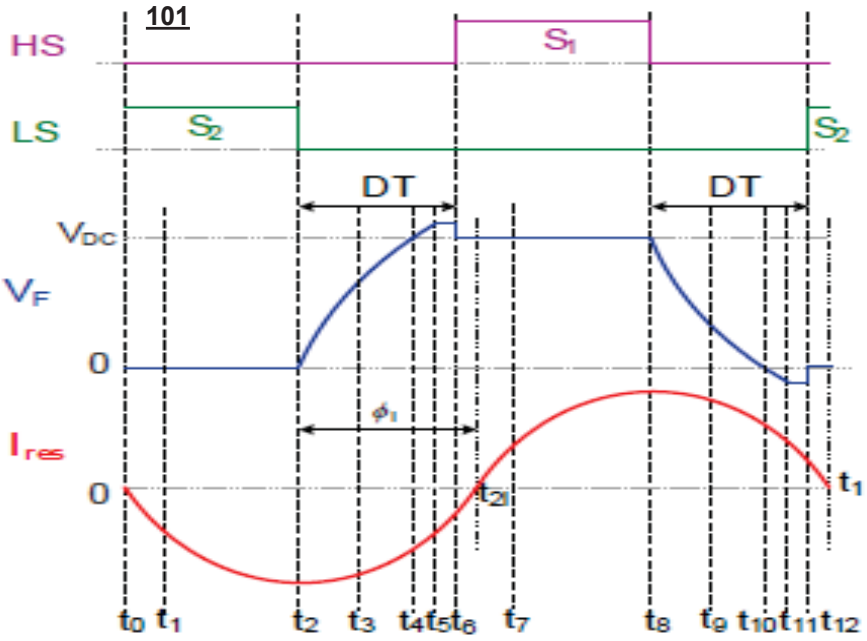
101
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S1
LS
S2
S2
DT
DT
VDC
VF
0
ϕ1
Ires
0
t2l
t1
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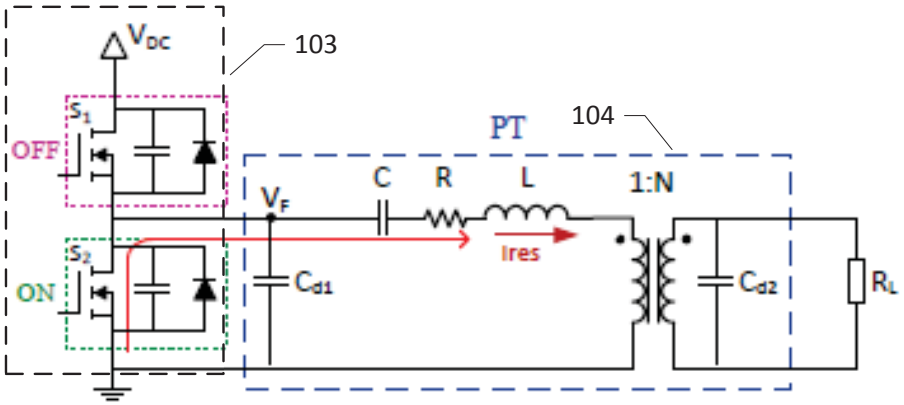
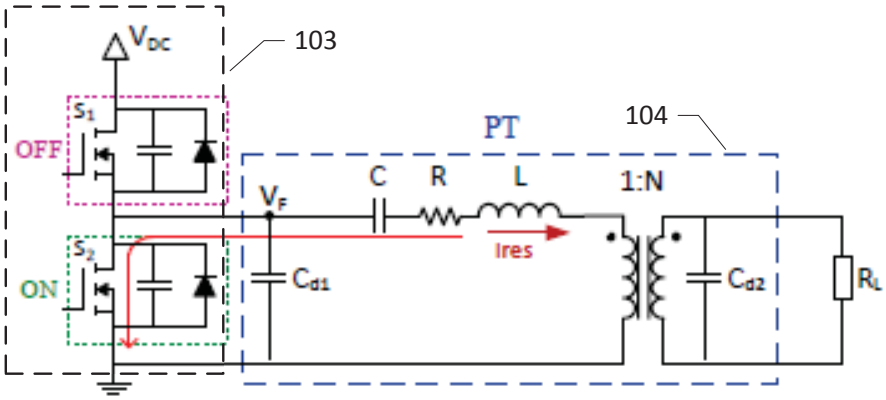
FIG. 1



a: Subinterval $t_{12} - t_{1f}$



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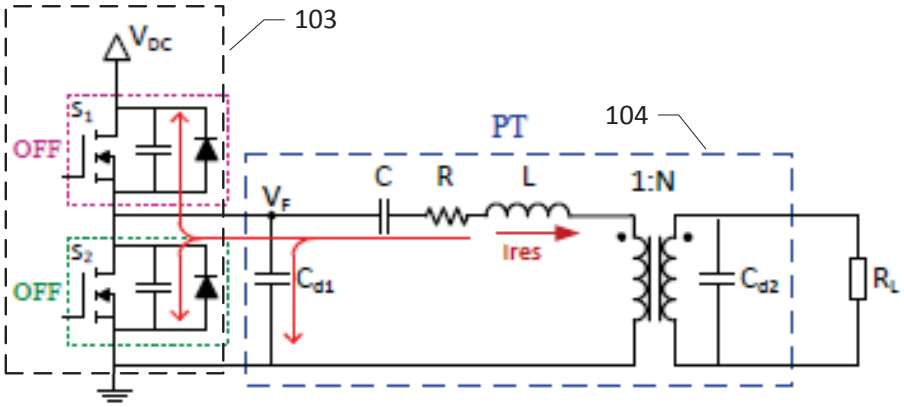
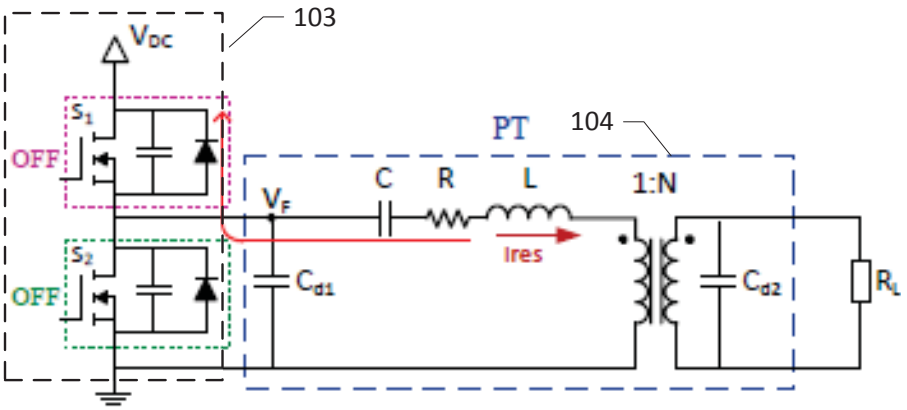
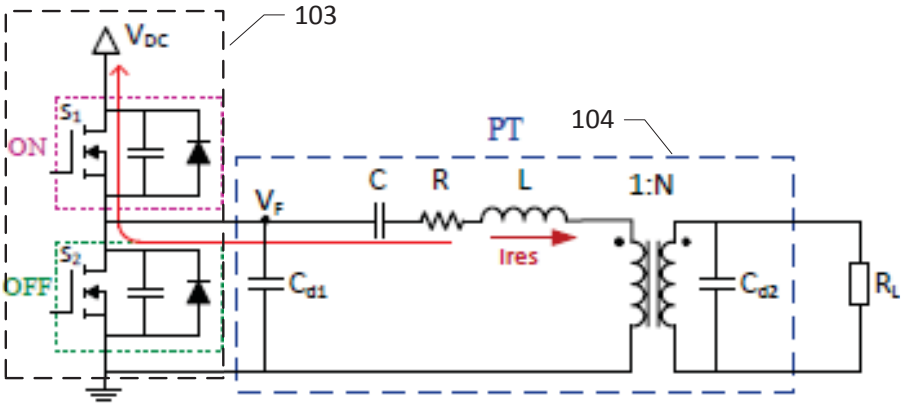


c: Subinterval $t_2 - t_5$

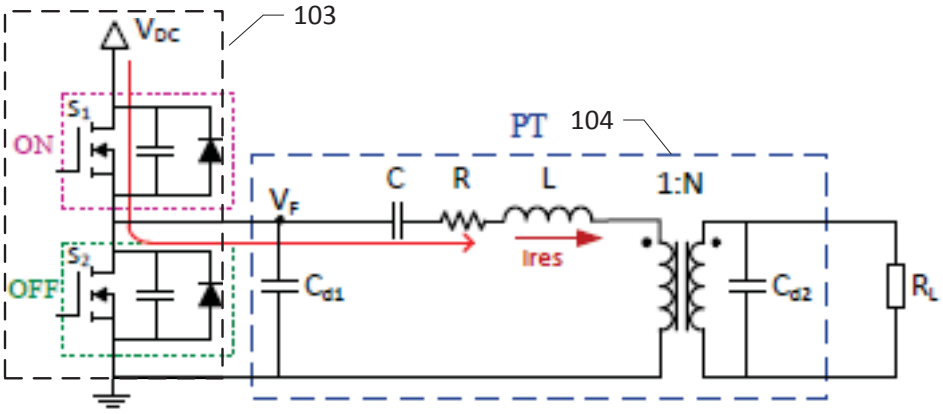
FIG. 1A



d: Subinterval $t_5 - t_6$

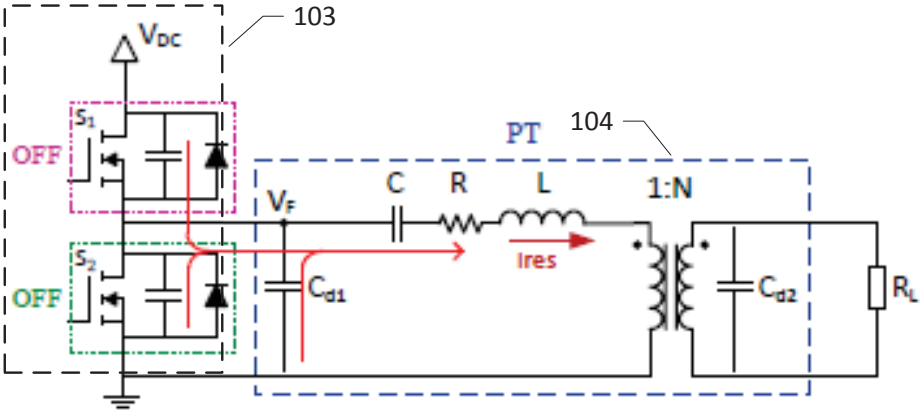


e: Subinterval $t_6 - t_{2I}$

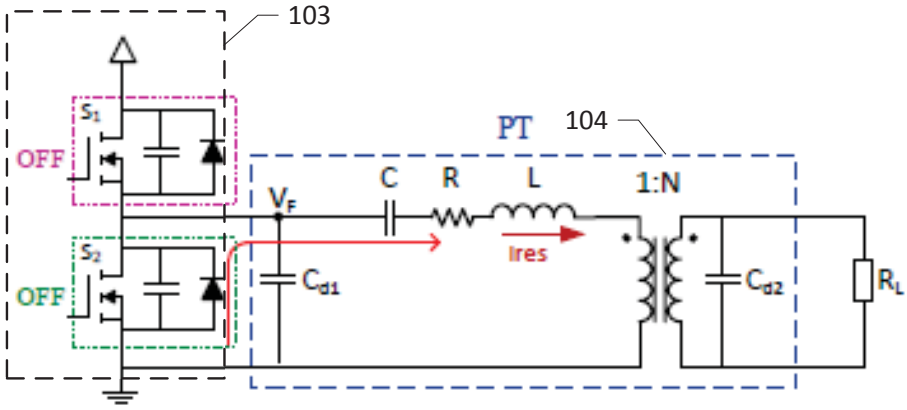


f: Subinterval $t_{2I} - t_8$

FIG. 1B

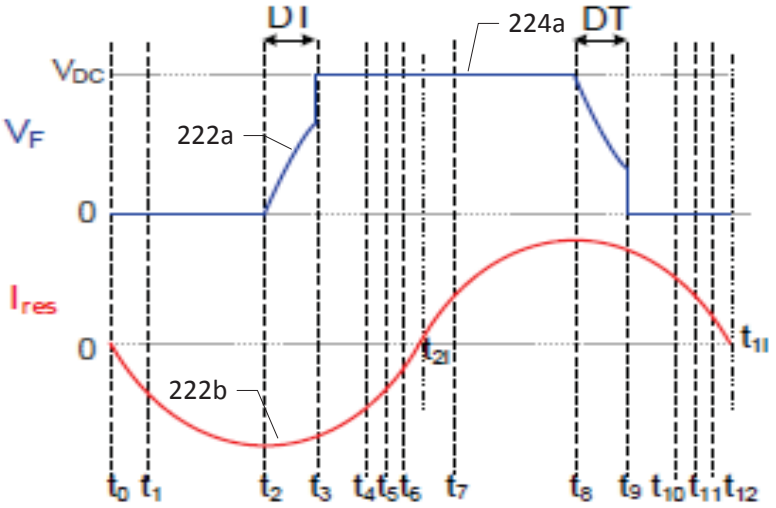


g: Subinterval $t_8 - t_{11}$



h: Subinterval $t_{11} - t_{12}$

FIG. 1C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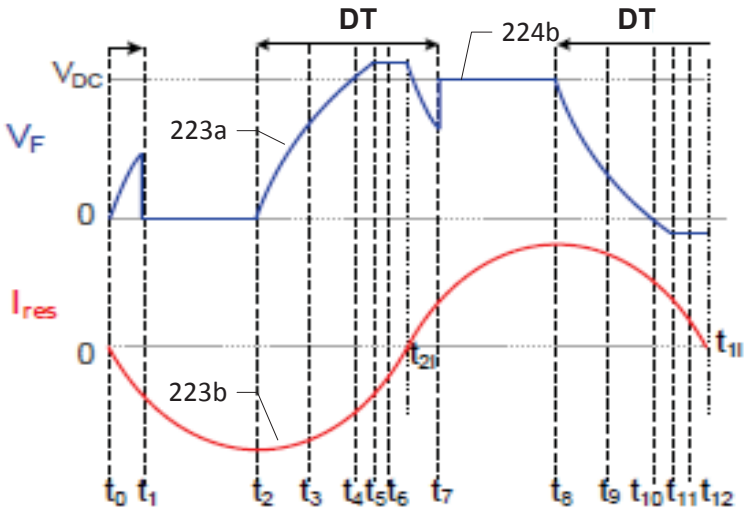
224a
DT
V_{DC}
V_F
222a
0
I_{res}
0
t_{2I}
t_{1I}
222b
t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9 t_{10} t_{11} t_{12}

A)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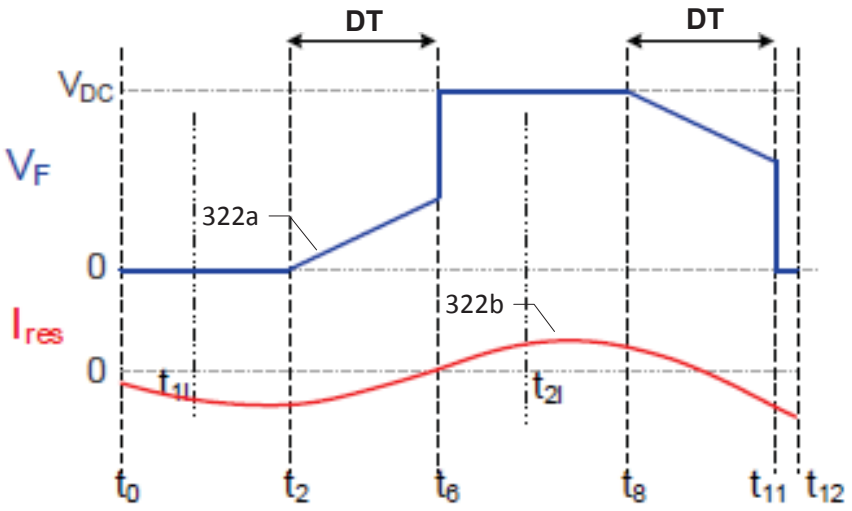
224b
DT
V_{DC}
V_F
223a
0
I_{res}
0
t_{2I}
t_{1I}
223b
t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9 t_{10} t_{11} t_{12}

B)

FIG. 2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DT
VDC
VF
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322b
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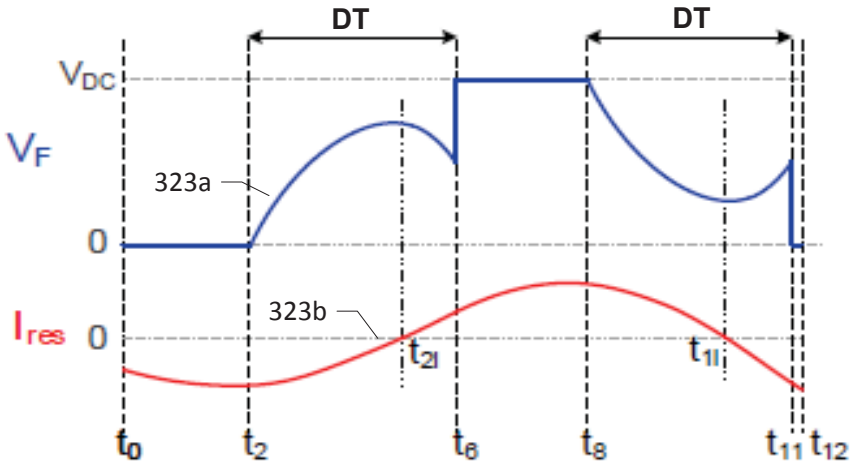
t2I
t0
t2
t6
t8
t11
t12

A)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DT
VDC
VF
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323b
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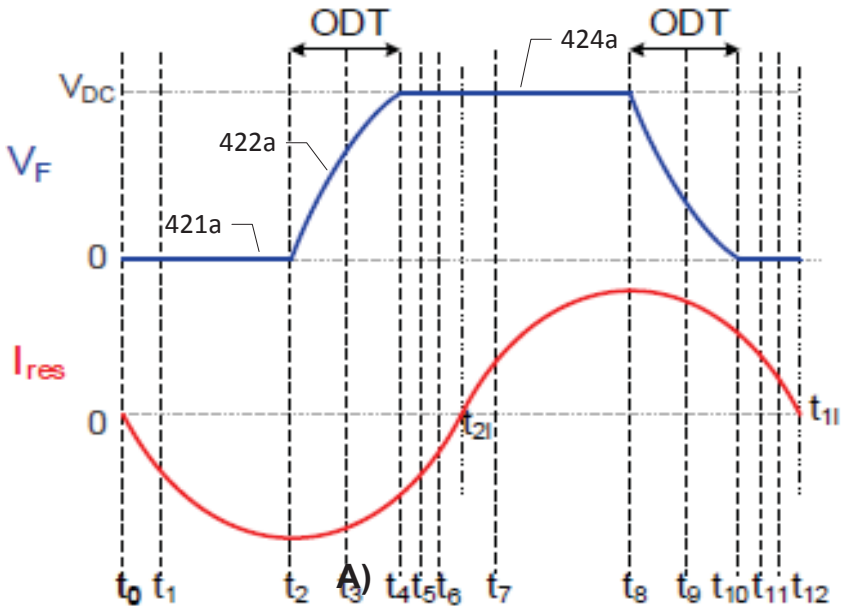
t1I
t0
t2
t6
t8
t11
t12

B)

FIG. 3


ODT
ODT
424a
V_{DC}
V_F
422a
421a
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0
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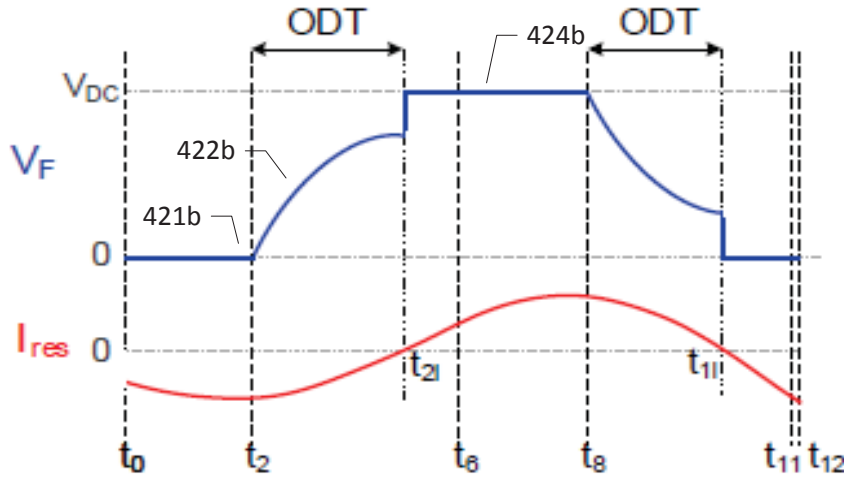
A)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V_F
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B)

FIG. 4

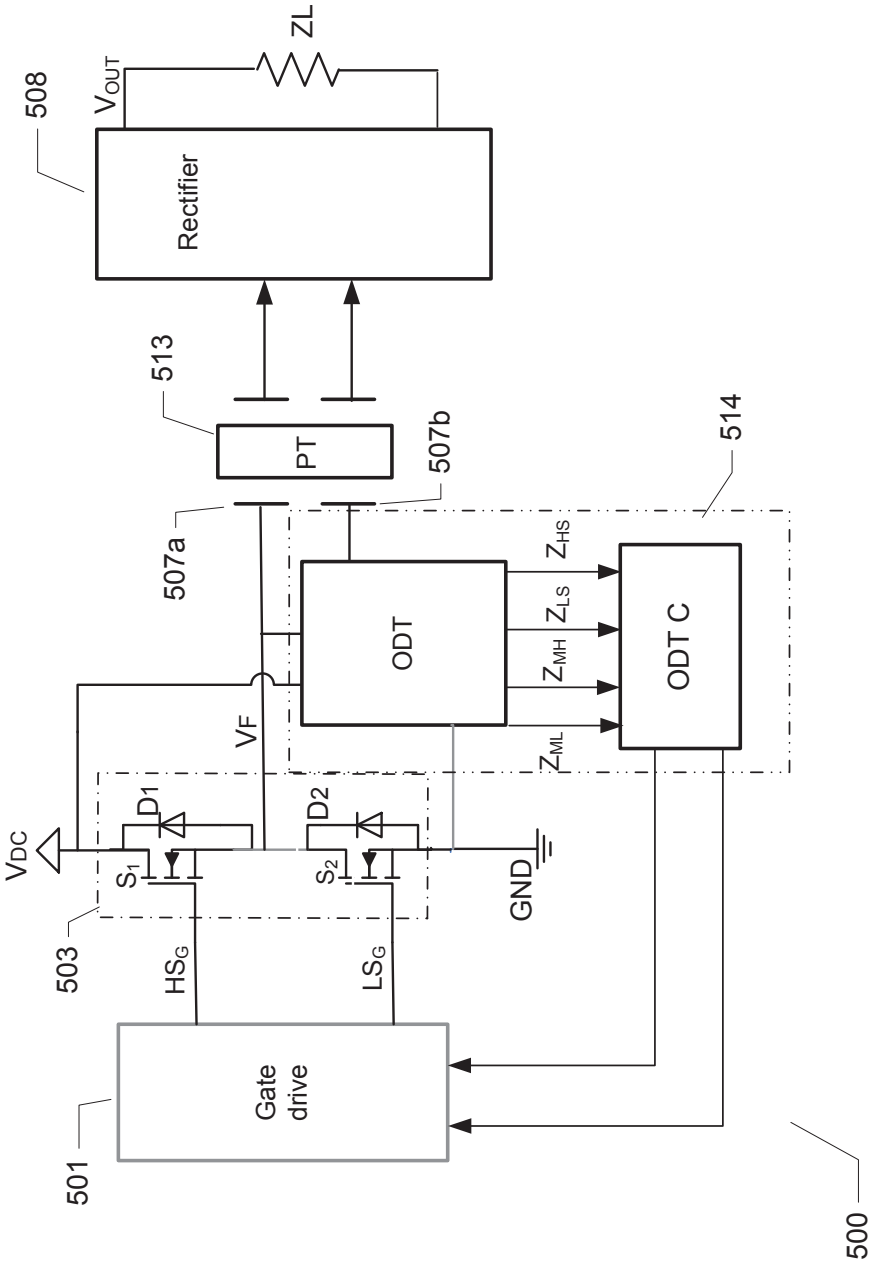
ZL
508
V_{OUT}
Rectifier
513
PT
507b
514
507a
ODT
Z_{HS}
Z_{LS}
Z_{MH}
Z_{ML}
ODT C
VF
D1
D2
V_{DC}
S_1
S_2
GND
503
HS_G
LS_G
Gate drive
501
500

FIG. 5

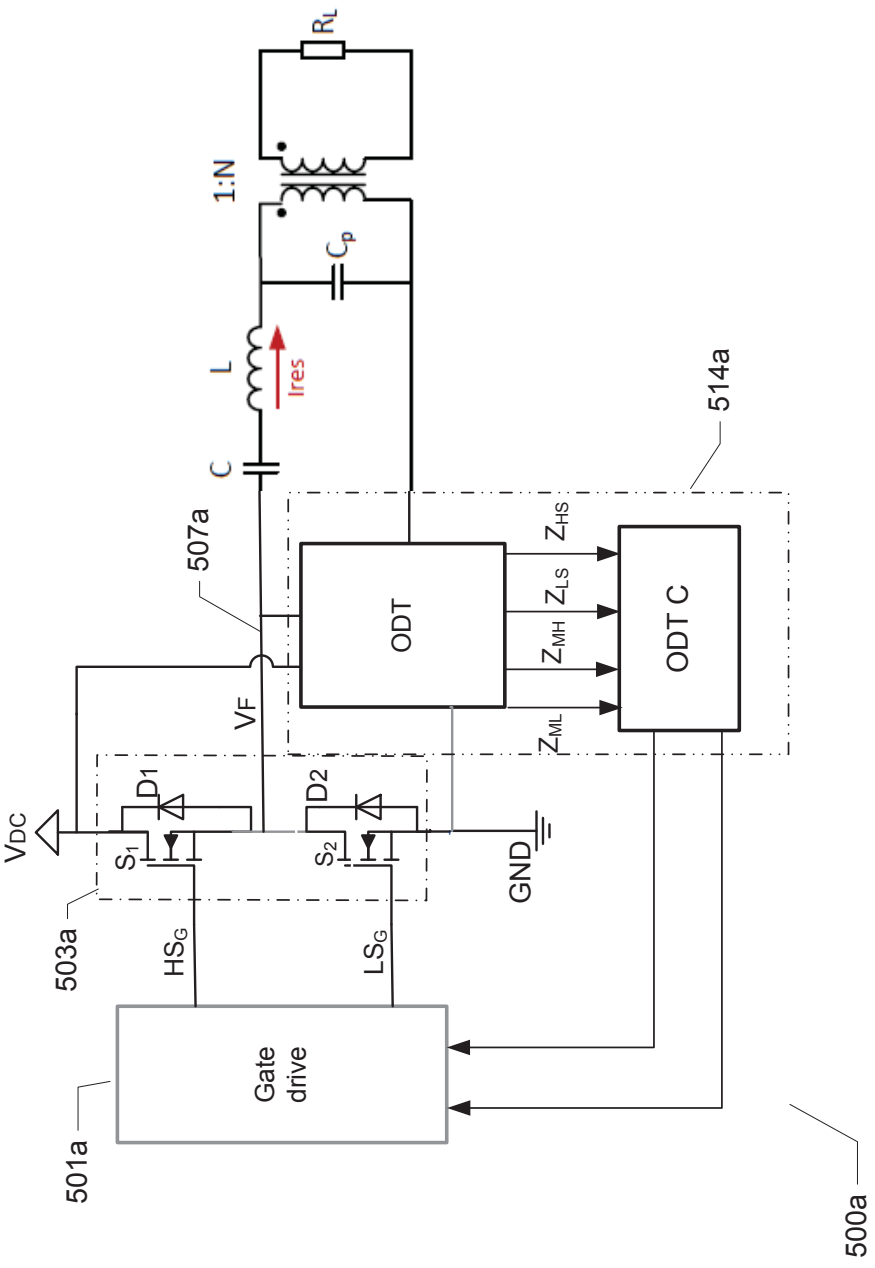
R_L
1:N
C_p
L
Ires
C
514a
507a
Z_{HS}
Z_{LS}
Z_{MH}
Z_{ML}
ODT
ODT C
VF
D1
D2
V_{DC}
S_1
S_2
GND
503a
HS_G
LS_G
Gate drive
501a
500a

FIG. 5A

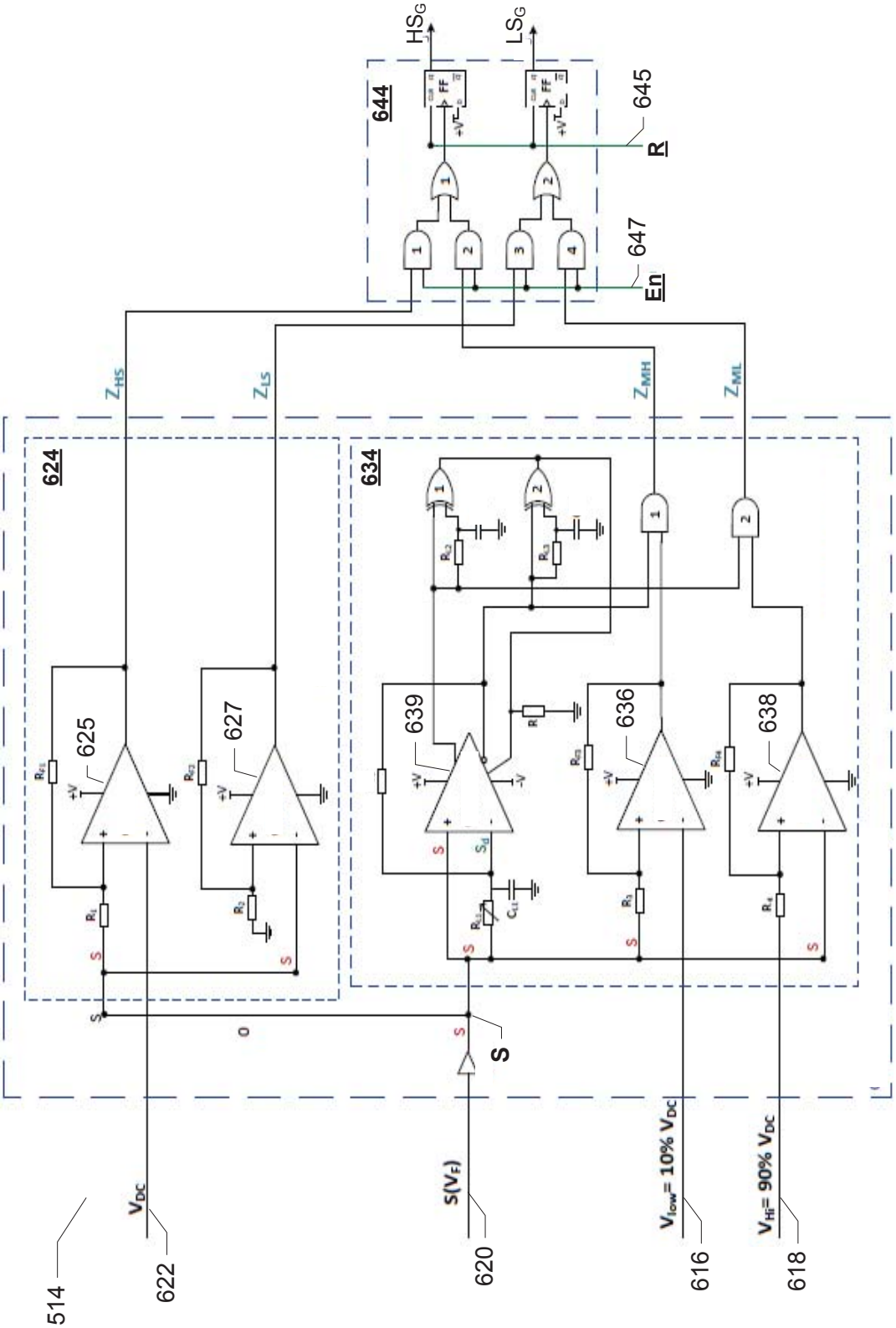
HSG
LSG
644
645
R
647
En
ZHS
ZLS
ZMH
ZML
624
634
625
627
639
636
638
S
S(VF)
VDC
Vlow= 10% VDC
VHi= 90% VDC
514
622
620
616
618

FIG. 6

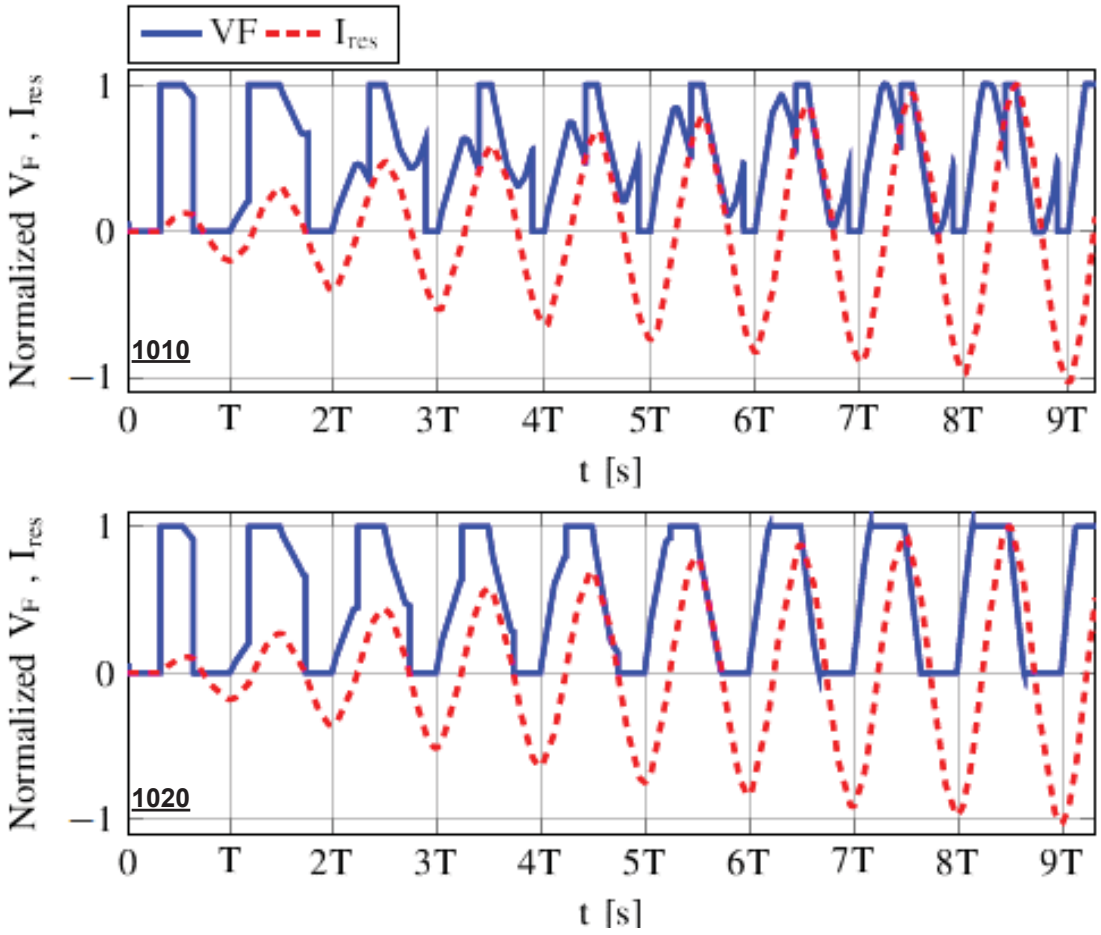
VF
I_{res}
Normalized V_F , I_{res}
1
0
−1
1010
0
T
2T
3T
4T
5T
6T
7T
8T
9T
t [s]
Normalized V_F , I_{res}
1
0
−1
1020
0
T
2T
3T
4T
5T
6T
7T
8T
9T
t [s]

FIG. 7

Appendix H

Analysis of bi-directional piezoelectric-based converters for zero-voltage switching

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Under review at

IEEE Transaction on Power Electronics IEEE-TPEL (2015)

Analysis of bi-directional piezoelectric-based converters for zero-voltage switching operation

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***Abstract*—This paper deals with a thorough analysis of zero-voltage switching especially for bi-directional, inductorless, piezoelectric transformer-based switch-mode power supplies with a half-bridge topology. Practically, obtaining zero-voltage switching for all of the switches in a bi-directional piezoelectric power converter is a difficult task. However, the analysis in this work will be convenient for overcoming this challenge. The analysis defines the zero-voltage region indicating the operating points whether or not soft switching can be met over the switching frequency and load range. For the first time, a comprehensive analysis is provided, which can be used as a design guideline for applying control techniques in order to drive switches in piezoelectric transformer-based converters. This study further conveys the proposed method to the region where all the switches can obtain soft switching. Moreover, the analysis can be applied to other types of resonant converters with or without piezoelectric transformers. Experimental and simulation results are provided, verifying the performed analysis.**

***Index Terms*—Resonant converter; zero-voltage switching; piezoelectric transformer; optimum dead time; phase shift control.**

NOMENCLATURE

v_{FP}	Switching voltage in the primary side of the transformer.
v_{FS}	Switching voltage in the secondary side of the transformer.
i_{res}	Resonant current of the piezoelectric transformer.
Φ_I	Phase shift of the resonant current with reference to the turn-off time of the low-side switch.
$\Phi_{ODT,P}$	Phase corresponding to the optimum dead time in the primary-side switching.
$\Phi_{ODT,S}$	Phase corresponding to the optimum dead time in the secondary-side switching.
C_{d1}	Input electrode capacitance of the piezoelectric transformer.
C_{d2}	Output electrode capacitance of the piezoelectric transformer.
C_{oss}	Output capacitance of MOSFETs or parasitic capacitance of rectifier's diodes.
C_{in}	Equivalent input capacitance of the piezoelectric transformer and switches.
C_{out}	Equivalent output capacitance of the piezoelectric transformer and switches.
NELIP	Normalized effective load impedance plane.
Z_p	Impedance seen from the inverter's switching node.
Z_s	Impedance seen from the rectifier's switching node.
Z_{np}	Effective impedance seen from the inverter's switching node.
R_{np}	Normalized effective real part of Z_{np}.
X_{np}	Normalized effective reactance of Z_{np}.
Z_{ns}	Effective impedance seen from the rectifier's switching node.
R_{ns}	Normalized effective real part of Z_{ns}.
X_{ns}	Normalized effective reactance of Z_{ns}.

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I. INTRODUCTION

Piezoelectric ceramic transformers (PTs) allow the replacement of magnetic transformers with a single ceramic component [1]. In some specific applications, e.g. with low cost, low size, low electromagnetic interference (EMI), PTs are preferred over electromagnetic transformers [2], [3]. PTs are initially considered as high-voltage transformer devices [2], [4]. This has rapidly increased the research and development within PT-based power converters [5]–[8] due to their high power density and high efficiency. Recently, inductorless PT-based switch-mode power supplies (SMPS) are used because of their specific usage in nonmagnetic applications [9]–[12]. The elimination of a bulky inductor reduces the size, weight, EMI, and cost [13].

A PT behaves as a resonant LC tank in its resonance frequency [13]. Therefore, PTs are employed to entirely replace the resonant network in resonant power converters. A resonant converter is simply composed of a switching network (i.e. an inverter), a resonant network, a rectifier network and a load. The block diagram of this system is shown in Fig. 1. The switching network can be either half-bridge or full-bridge configuration. The resonant network is classified as resonant tank or PT. A variety of resonant tanks can be employed i.e. a series resonant tank comprised of series LC, parallel resonant tank comprised of parallel LC tank, LLC or LCC tank networks [14]–[17]. The rectifier network is either passive [15], [18] or active, comprised of a diode rectifier network or switching network. In order to increase the converter's efficiency, it is particularly important to operate the converter in the desired operating points, where zero-voltage switching (ZVS) is ensured. However, the conditions for achieving ZVS varies with temperature, the load and the switching frequency [5], [19], [20]. Therefore, it is desirable to find the frequency range and the load variations in which ZVS can still be obtained [21]. However, PT-based resonant converters are typically operated with a switching frequency to have an inductive impedance seen from switching node

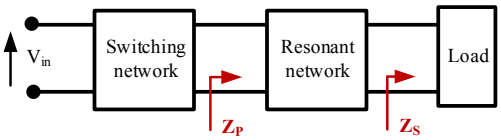


Fig. 1: A simple block diagram of a resonant converter.

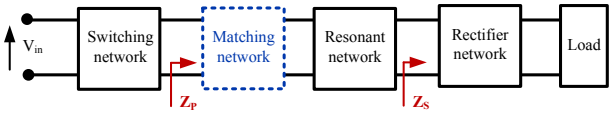


Fig. 2: A simple block diagram of a resonant converter.

(Z_P) [12], [22], [23], but this does not ensure the achievement of ZVS [24]. Furtheremore, characteristics of the PT should allow for obtaining soft switching [5], [22]. Several attempts have been made to express the soft switching capability especially for PTs with some limitations [5], [25].

The commonly used solution is to add a matching network between the switching network and the resonant network, as shown in Fig. 2. The load-source matching networks can be designed to shift the operating point to the area where ZVS is attained. In the most cases this is done by utilizing an additional series inductor between the switching network and the resonant network [4], [26]. Moreover, the matching network usually consists of an inductor, which is not a suitable solution for the inductorless converter topologies, due to its nonmagnetic applications [9]. This thereby brings some limitations to utilizing the solution of matching network.

Another solution within the PT-based SMPS is to have a PT which is inherently capable of obtaining soft switching. This requires several conditions to be fulfilled in the design of the PT [5] for a certain load. There is a narrow frequency band within which the PT shows an inductive characteristic [27]. Therefore, achieving ZVS for the PT-based driver under various range of loads is quite challenging [9], [22], [23], [26].

To date there are literatures about ZVS, but not specifically for power converters with piezoelectric transformers. However, existing solutions can be utilized for PT-based converters in a limited operating conditions. The analysis in this paper, extends the ZVS region and conditions for attaining ZVS to a broader range. The goal of this paper is to investigate the PT-based converter's operating points to meet soft switching both for the inverter and the rectifier networks. The investigation performed in this paper can be generalized for all types of resonant converters, even though the discussion focuses on PT-based converters. The main purpose is to find a simplified equivalent impedance seen from the switching node to find the ZVS region. Ultimately, the method represented in this paper can help overcome the limitations in control technology of PT-based drivers [28]. Furthermore, this work gives an estimation on the value of the minimum required dead time (DT) under the soft switching condition. Obtaining the minimum or optimum DT results in an efficiency increase of the converter. The proposed converter can be used for energy recovery from the capacitive loads, e.g. piezo actuators (PA) in [9] and [26], Dielectric electro active polymers (DEAP) actuators in [28]. Moreover, the application of this paper is not limited to the PT-based converters. It can be applied for other type of resonant converters as are named in this Section. Implementation of energy recovery strategies will be the key to obtain a highly efficient converter system which imposes strict requirements on advanced control schemes. This work help on understanding the concept through analysis in order to imply advanced control strategy for different applications.

The paper is organized as follows. Section II deals with the half-bridge rectifier network. Subsection II-A is dedicated to a description of a bi-directional converter's topology and related waveforms for a general case. The description is followed by analysis of active rectifier network in Subsection II-B. Section III describes a zero-voltage switching region specifically for the inverter network. Furthermore, analysis of waveforms is performed for the primary-side switches in Subsection III-A and for defining the ZVS-boundary in Subsection III-B. This analysis generally leads to the ZVS region and the optimum DT for the PT-based converters. Following this, analysis of the ZVS region is carried out in Section IV for the rectifier network. The description is followed by analysis for a passive rectifier network in Subsection IV-B and its boundary in Subsection IV-A. A short discussion follows in Subsection IV-D about the equivalent resistor of the output network for the resonant converters with series resonant tank. Experimental and simulation results are provided in Subsections III-C and IV-C.

II. PT-BASED SMPS WITH HALF-BRIDGE RECTIFIER NETWORK

The half-bridge PT-based SMPS operates similar to the true Class DE inverter studied in [29]. In addition to previous research, this paper investigates the large-scope operation of waveforms and ZVS region for the uni-directional and bi-directional topologies. The analytical method was inspired from the principle of equivalent impedances Z_P and Z_S through Fourier analysis [30], employed to determine the ZVS region. The Z_P is seen from the switching network and Z_S is seen from input of the active rectifier network. In the PT-based SMPS, the input capacitance and the output capacitance of the PT, in parallel with the output capacitances of the switches, should be fully charged and discharged for attaining ZVS. Since the input and output capacitance of PTs are typically larger than the output capacitances of metal-oxide-semiconductor field-effect transistors (MOSFETs), achieving ZVS is more challenging in these kinds of converters compared to class DE converters. Presently, bi-directional topology is not commonly used in PT-based converters. Therefore, the purpose of this work is to give a comprehensive analysis for the bi-directional functionality of PT-based SMPS.

A. Bi-directional topology

Bi-directional PT-based SMPS with the active half-bridge rectifier shown in Fig. 3 and is studied in this work. Fig. 4 shows bi-directional prototype built and used for experimental results in this work. The following analysis focuses on finding equivalent impedances Z_P and Z_S shown in Fig. 3. The resonant current is dependent on the resonant components in

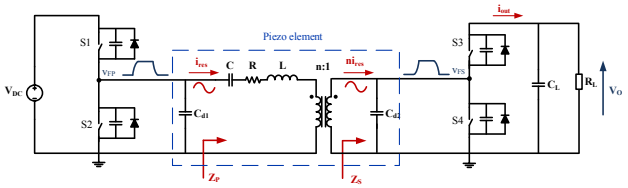


Fig. 3: Bi-directional PT-based switch-mode power supply.The Mason's lumped parameter model is used for PT [31]–[33].

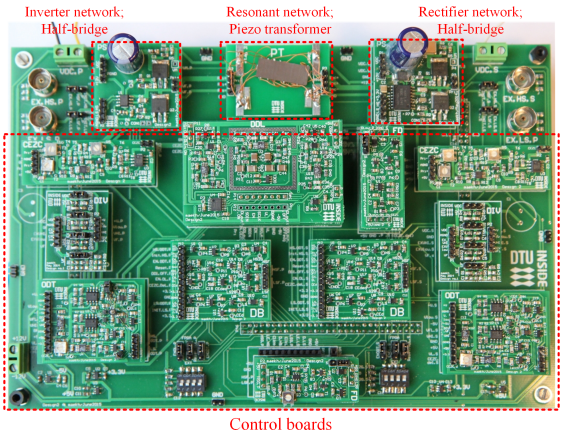


Fig. 4: The prototype of bi-directional PT-based switch-mode power supply.

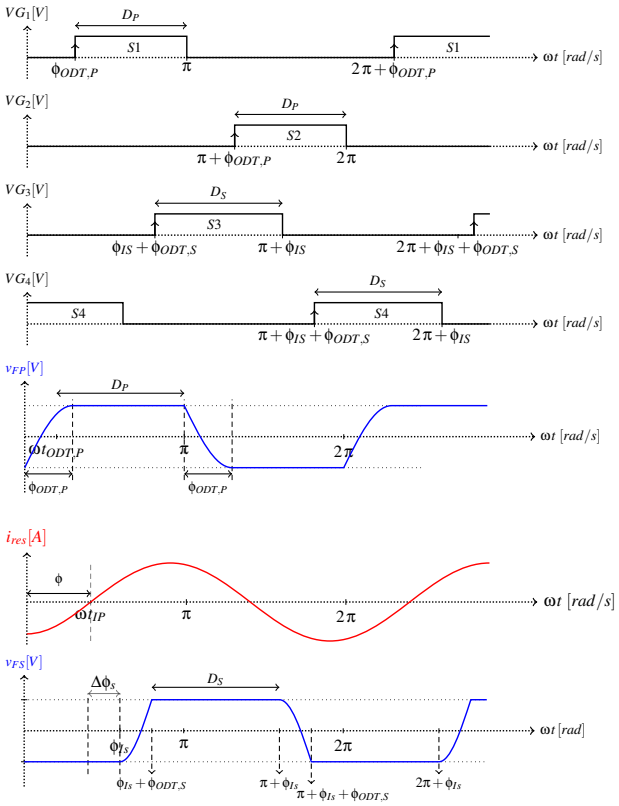


Fig. 5: Waveforms in the bi-directional topology: Gate voltage of switches, resonant current i_{res} and switching voltages of the inverter v_{FP} and the rectifier v_{FS}.

the resonant network as well as the load. The impedance Z_S is the equivalent impedance of the rectifier network together with the load. Therefore, Z_S is also load dependent. In other words, changes in the load, make changes in the impedance seen from the output of the PT. This causes changes in the phase and the amplitude of the resonant current. Consequently, changes in the load convert to the equivalent impedance seen from the switching node, Z_P. Principally, the impedance Z_P, which is calculated in Section III, is dependent on the load, the switching frequency, and the phase shift between the resonant current and the fundamental component of the switching voltage. This then helps us to find the ZVS region for the switching network. For simplicity, the following analysis is based on the following assumptions that do not affect the general aspect of the results:

- The converter's input capacitor is considered as a summation of the PT's input capacitance and both MOSFET's output capacitances in the switching network:

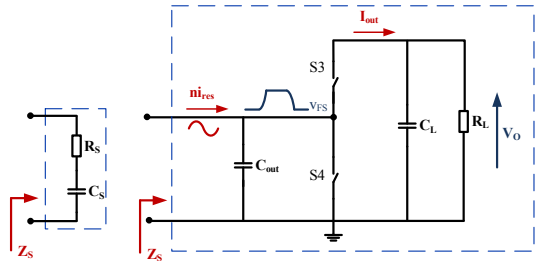
$$C_{in} = C_{d1} + 2\,C_{oss} \tag{1}$$

- The converter's output capacitor is considered as a summation of the PT's output capacitance and both MOSFET's output capacitances in the rectifier network:

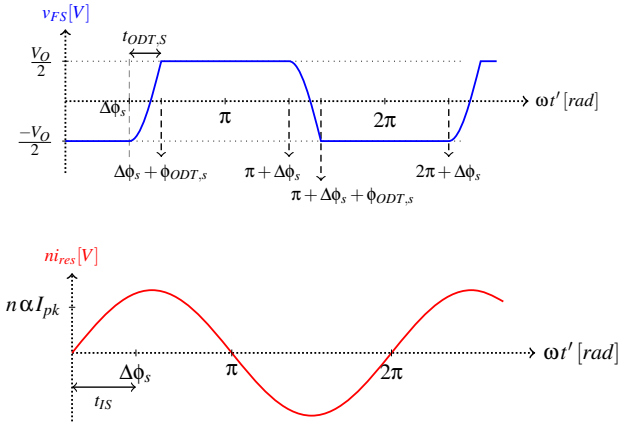
$$C_{out} = C_{d2} + 2\,C_{oss} \tag{2}$$

- The load capacitor is large enough to keep the output voltage in a constant level without any ripple.
- The temperature of the PT remains constant.

Fig. 5 shows overall waveforms for the inductorless PT-based SMPS. Utilizing an active rectifier allows for having an active phase shift between the rectifier switches and the inverter switches that consequently enables a bi-directional power flow [23]. In order to have full control of the power flow in the bi-directional mode, the key is to control the phase shift between the two switching networks, $\phi + \Delta\phi_s$. Moreover, the target is to have ZVS for the switches on both primary- and secondary-sides of the PT to improve the efficiency. In order to achieve ZVS, the gate voltages of the switches should allow for the voltage v_{FP} to lead the resonant current and the voltage v_{FS} to lag the resonant current. Applying an amount of the phase shift, $\Delta\phi_s$, allows for changes in the power flow and ultimately changes the level of the output voltage. This change further causes changes in the amplitude and the phase shift of the resonant current, ϕ. Consequently, this affects the time span where the switching voltage transits between the rails, which is called minimum or optimum DT under the ZVS condition. Moreover, it is important to investigate the operating points that rectifier network or the inverter network can achieve ZVS for each output voltage level. Accordingly, this work analyzes the comprehensive situation for variations of $\Delta\phi_s$ versus ϕ and suggests the optimum DT for obtaining ZVS.



(a) Electrical equivalent circuit.



(b) Signal waveforms.

Fig. 6: Output circuit of the converter with active rectifier. Waveforms: resonant current i_{res} and floating voltage v_{FS} in the general state.

B. The converter's output characteristic

In the following analysis, for simplicity, the normalized time axis is changed to $\omega t'$ where $\omega t' = \omega t - \phi$. Thereby, the resonant current is considered with zero phase shift. There is a phase shift between the current and the time where the low-side switch is turned off, which is defined as $\Delta\phi_S$.

$$i_{res}(t') = I_{pk}\, sin(\omega t') \tag{3}$$

The output voltage is found as:

$$V_o = \frac{2nR_L I_{pk}\, cos(\Delta\phi_s)}{2\pi + R_{Ln}} \tag{4}$$

where, $R_{Ln} = \omega R_L C_{out}$ is a normalized load resistance. Hence, the output power will be

$$P_{out} = \frac{4}{R_L}\left(\frac{nI_{pk}\, cos(\Delta\phi_s)}{2\pi + R_{Ln}}\right)^2 \tag{5}$$

The normalized impedances seen from the rectifier's floating point is $Z_{ns} = R_{ns} + jX_{ns}$, where the effective real part is

$$R_{ns} = \frac{8R_{Ln}\cos^2(\Delta\phi_s)}{(2\pi + R_{Ln})^2} \tag{6}$$

and the effective reactance is described as

$$X_{ns} = \frac{A}{\pi}\frac{2\pi - R_{Ln}}{(2\pi + R_{Ln})^2}\, cos(\Delta\phi_s) - \frac{1}{\pi}\left(\phi_{ODT,S} + sin(2\Delta\phi_s)\right) \tag{7}$$

from Equation (4), $\Delta\phi_s$ can be derived as a factor of other parameters.

$$\Delta\phi_s = cos^{-1}\left(\frac{V_o}{2nR_L I_{pk}}(2\pi + R_{Ln})\right) \tag{8}$$

Equation (8) gives a relationship to calculate the required phase shift of the rectifier switches, $\Delta\phi_s$, for the voltage level of V_o over the switching frequency of ω and load of R_L. The following equations will be further discussed in Section IV regarding the ZVS region for the rectifier. More details about finding R_{ns} and X_{ns} are described in the appendix.

III. ZVS for the Inverter Network

A. Analysis of impedance Z_P

Fig. 7 shows the input circuit of the converter and the related waveforms; the floating voltage v_{FP} and the resonant current (i_{res}), which are studied in detail in the following analysis. Since piezo transformers have a high quality factor [34], higher harmonics are filtered out and only the fundamental component of the current passes through the output [27], [35]. Therefore, the resonant current is a sinusoidal waveform with a peak amplitude of I_{pk} and a phase shift of ϕ.

$$i_{res}(t) = I_{pk}\, sin(\omega t\ -\ \phi) \tag{9}$$

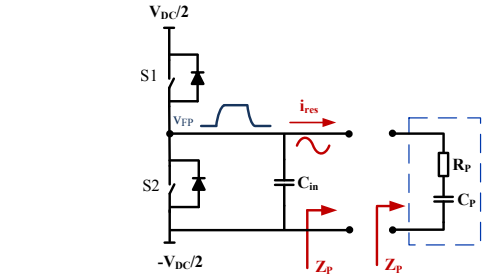
where, ϕ is phase shift between resonant current and the turn-off time of the low-side switch, $S2$, described by Equation (10). At the time point $t_{ODT,P}$, the floating voltage v_{FP} transits between voltage rails. The resonant current changes its direction when the high-side switch conducts; either S1 is turned on or its body diodes clamps. Therefore, $\phi \geqq \phi_{ODT,P}$.

$$\phi = \omega t_{IP} \qquad \phi \in [0, \pi] \tag{10}$$

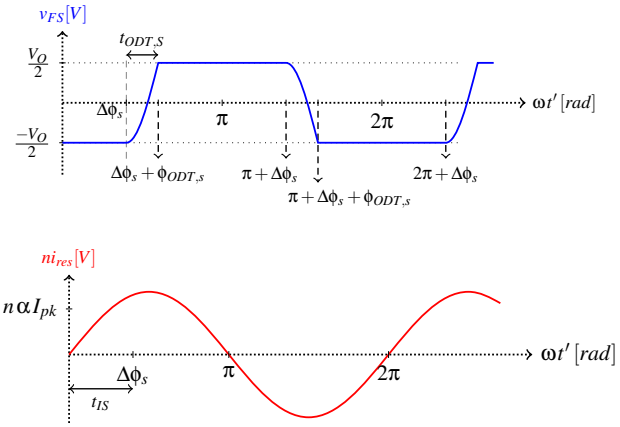
$$\phi_{ODT,P} = \omega\, t_{ODT,P} \qquad \phi_{ODT,P} \in [0, \pi] \qquad \text{and } \phi_{ODT,P} \leqslant \phi \tag{11}$$

For convenience, the dc input is shown as a center-taped supply. This eases finding the Fourier components by applying symmetry to the waveforms. When the low-side switch is turned off at $t = 0$, both switches $S2$ and $S1$ are off. The resonant current keeps its direction in the reverse orientation charging the input capacitance C_{in} to the positive rail. The optimum DT, t_{ODT}, is defined as the time when the voltage across C_{in}, v_{FP}, reaches to $V_{DC}/2$. At this time point, the high-side switch $S1$ is turned on before its body diode starts to conduct. This further prevents unnecessary dead time between the switches and consequently, efficiency increment. Normalized input impedance seen from the inverter's floating point is found as $Z_{np} = R_{np} + jX_{np}$, where the effective real part and the effective reactance is described as (12) and (13)

$$\begin{aligned} R_{np} = \frac{-1}{\pi}\Big[&\frac{-1}{2}\, sin(2\,\phi_{ODT,P} - \phi)\, sin(\phi)\ -\ \frac{1}{2}sin^2(\phi) \\ &+ \phi_{ODT,P}\, sin(\phi)\, cos(\phi_{ODT,P}) - \phi_{ODT,P}\, cos(\phi)\, sin(\phi_{ODT,P}) \\ &-\ \frac{1}{2}\, cos(2\,\phi_{ODT,P} - \phi)\, cos(\phi)\ +\ \frac{1}{2}cos^2(\phi)\Big] \end{aligned} \tag{12}$$



(a) Electrical equivalent circuit.



(b) Signal waveforms i_{res} and v_{FP}.

Fig. 7: Primary-side of the SMPS considering general operation where the resonant current and the input floating voltage have phase shift of ϕ.

$$X_{np} = \frac{-1}{\pi}\,[\,-\phi_{ODT,P}\,sin(\phi_{ODT,P})sin(\phi) - \frac{1}{2}cos(2\,\phi_{ODT,P} - \phi)\,sin(\phi) + \frac{1}{2}\,cos(\phi)\,sin(\phi) + \frac{1}{2}\,cos(\phi)\,sin(2\,\phi_{ODT,P} - \phi) + \frac{1}{2}\,sin(\phi)cos(\phi) - \phi_{ODT,P}cos(\phi)\,cos(\phi_{ODT,P})] \tag{13}$$

The inverter's switches operate with a duty cycle of $D_P \in [0,0.5]$;

$$D_P = \frac{\pi - \phi_{ODT,P}}{2\pi} \tag{14}$$

Details for finding Z_{np} are described in the appendix.

B. ZVS region boundary for the inverter

The resonant current has a phase shift with the floating voltage, which varies with the parameters of the piezo transformer and the load. For operating points located on the boundary of ZVS region, the resonant current crosses zero when the v_{FP} reaches the rails at its peak value. This means that the voltage across the input capacitor C_{in} reaches its peak value at the optimum dead time. Therefore, $dv_{FP}/dt = 0$ at $t_{ODT,P}$. This occurs when the resonant current crosses zero and consequently $\phi = \phi_{ODT,P}$. Substituting $\phi_{ODT,P} = \phi$ into Equations (12) and (13) results in the following equations.

$$R_{nP,B} = \frac{1}{\pi}\,[\,sin^2(\phi)] \tag{15}$$

$$X_{nP,B} = \frac{-1}{\pi}\,[\,-\phi + sin(\phi)\,cos(\phi)] \tag{16}$$

The duty cycle of the switches in this case is:

$$D_{P,B} = \frac{\pi - \phi}{2\pi} \tag{17}$$

The complex impedance plane of Z_{np} which is the $R_{np} - X_{np}$ plane named as the normalized effective load impedance plane (NELIP) in Fig. 8. The Locus of ZVS is shown in the NELIP. The boundary of the ZVS region shows the case where the voltage across C_{in} reaches the positive rail at its peak value. The boundary of ZVS region in the NELIP plane is designated by the operating points $R_{nP,B}$ and $X_{nP,B}$ which are shown by a cycloid defined as:

$$X_{nP,B} = r\cos^{-1}\left(1 - \frac{R_{nP,B}}{r}\right) - \sqrt{R_{nP,B}\,(2r - R_{nP,B})} \tag{18}$$

This cycloid is the locus of a point on the rim of a circle of radius r rolling along the X_{np} axis, where $r = 1/2\pi$. The arch of cycloid is shown in Fig. 8 which is closed by a line across X_{np}. In this case, the amplitude of the resonant current is:

$$I_{pk,B} = \frac{V_{DC}\,\omega C_{in}}{1 - cos(\phi)} \tag{19}$$

Therefore, I_{pk} for any case can be defined as a multiple factor of $I_{pk,B}$ by the factor of α.

$$I_{pk} = \alpha I_{pk,B} \tag{20}$$

The equivalent impedance, Z_{pe}, of the converter seen from the switching node of the inverter is dependent on the load, output voltage and the duty cycle of the rectifier. The ZVS region is found by comparing this equivalent impedance in all cases to the critical case located on the cycloid. Therefore, two cases where Z_{pe} is located inside and outside of the NELIP plane are described as follows:

- Inside the ZVS region: In the case that Z_{pe} has small values,α will be greater than 1, $\alpha > 1$, and $I_{pk} \geq I_{pk,B}$. In this situation the effective impedance is located inside the ZVS region, shown as the filled gray area in Fig. 8 bounded by the cycloid and the X_{np} axis. Therefore, the switching voltage v_{FP} reaches the rails before the zero crossing of the resonant current, and consequently, $\phi_{ODT,P} < \phi$. Hence, the duty factor of the switches, D_P, can be increased by detecting the optimum DT which means turning on the switches $S2$ and $S1$ at $t_{ODT,P}$ and $T/2 + t_{ODT,P}$, respectively. Therefore, the converter's efficiency increases due to ZVS operation. For resonant converters there is access to measure the amplitude and phase of the resonant current and thereby, the optimum DT is found as:

$$\phi_{ODT,P} = \phi - \cos^{-1}\left(\frac{1 + (\alpha - 1)\,cos(\phi)}{\alpha}\right) \tag{21}$$

In the PT-based converters typically there is no access

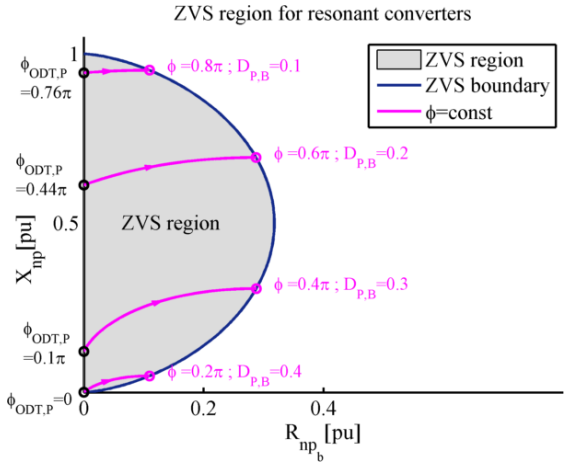


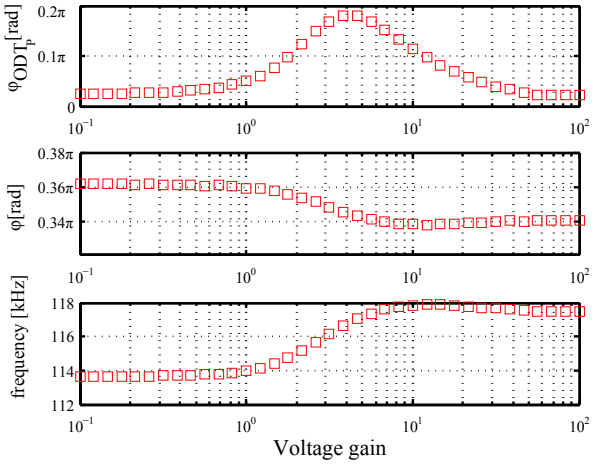
Fig. 8: Zero-voltage switching region.

to the resonant current inside the transformer package. Therefore, application of this equation is limited in practice for PT-based converters.

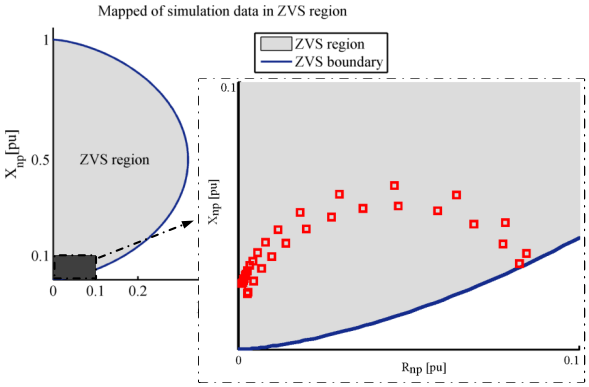
- Outside the ZVS region: This is the region of operating points for which the effective impedance is located outside the gray area. This occurs when Z_{pe} has large values and $\alpha < 1$. This means that the amplitude of the resonant current is not large enough to charge the input capacitance of the PT, C_{in}, to the positive rail. Therefore, zero voltage switching cannot be attained.

C. Inverter's results

Fig. 8 shows mapping of the NELIP plane. Additionally, the curves show maps of points inside the ZVS region from the equations in Section III. Points marked from each curve and located on the boundary of ZVS region can also be found by substituting $\phi_{ODT} = \phi$ in the equations provided in Subsection III-A. For instance if $\phi = 0.6\pi$, the $\phi_{ODT,P}$ can vary from 0.44π to 0.6π depending on the amplitude of the resonant current. In the case of resonant converters with discrete resonant tanks such as LC, LLC and LCC, there is access to measure the amplitude and phase of the resonant current. Therefore, the phase of the optimum dead time, $\phi_{ODT,P}$, is found from the related equations, and it corresponds to one of the points inside the NELIP. However, there is no access to sense the amplitude and phase of the resonant current inside the piezo transformers, but the analysis can be used to estimate the range of the optimum DT. Simulation results are shown in Fig. 9 for the half-bridge diode rectifier PT-based converter. These results show how the frequency, the phase shift of the resonant current and the optimum DT change when the voltage gain varies where ZVS is obtained. Furthermore, all the points are mapped in the NELIP plane. They are well situated inside the ZVS region by substituting in Equations (12) and (13). Fig. 10 shows experimental results for two operating points in the PT-base SMPS. Fig. 10a shows v_{FP} when the load of the PT is resistive. This operating point is mapped in P_1 in the NELIP plane in Fig. 10c. Fig. 10b shows v_{FP} when the load



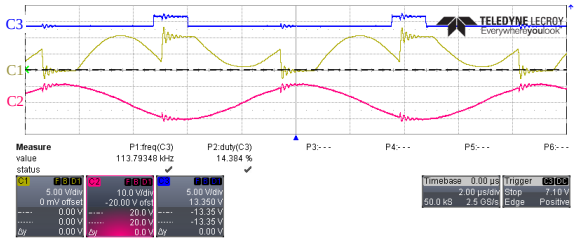
(a) Simulation data points, $V_{in} = 10V$.



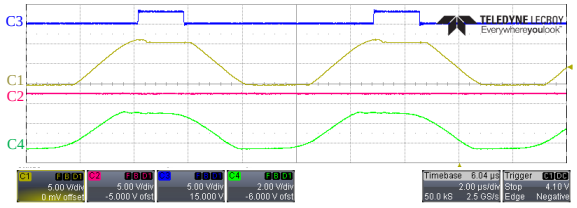
(b) Mapped of operating points in the inverter's NELIP.

Fig. 9: Simulation data of PT-based converter with a diode rectifier.

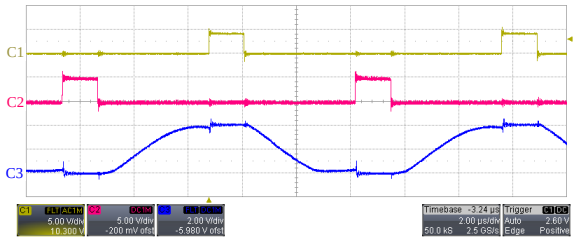
of the PT is passive rectifier. This operating point is mapped in P_2 in the NELIP plane (Fig. 10c.). In both cases a large DT is chosen in order to see the local peak of the voltage. As previously mentioned, the voltage v_{FP} passes through its peak when the resonant current crosses zero. Therefore, the phase of the resonant current, ϕ, is measured. The phase corresponding to the time that v_{FP} reaches the positive rail is measured as $\phi_{ODT,P}$. P_1 and P_2 are mapped by substituting the measured values into Equations (12) and (13). Experimental waveforms show that ZVS is attained and in the NELIP plane P_1 and P_2 are also located inside the ZVS region. The measured values are shown in Table I. For P_2 the measured value for $\phi_{ODT,P}$ is $0.54\,\pi$, which is in the range of $[0.35\,\pi, 0.55\,\pi]$ shown by the curve for possible operating points positioned on the curve, where the phase of the resonant current is $\phi = 0.55\,\pi$. Furthermore, the points $P_{1,B}$ and $P_{2,B}$ located on the boundary of NELIP plane show the case explained in Subsection III-B.



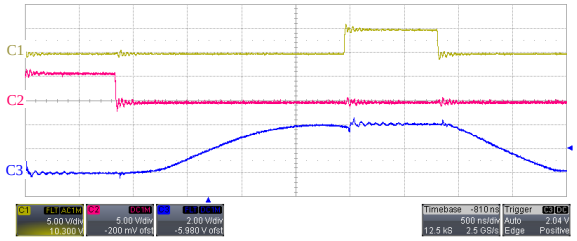
(a) An operating point (P1) for the PT-based converter with resistive load with $V_{in} = 10V$, frequency= $113.8kHz$, $R_L = 775\Omega$. C1: Inverter's switching voltage v_{FP}; C2: Output voltage of the converter with resistive load; C3: Gate voltage of the S1.



(b) An operating point (P2) for the PT-based converter with half-bridge diode rectifier with $V_{in} = 10V$, frequency= $114.8kHz$, $R_L = 100\Omega$, $V_o = 2.5V$. C1: Inverter's switching voltage v_{FP}; C2: Output voltage V_o; C3: Gate voltage of the S1; C4: Rectifier's switching voltage v_{FS}.



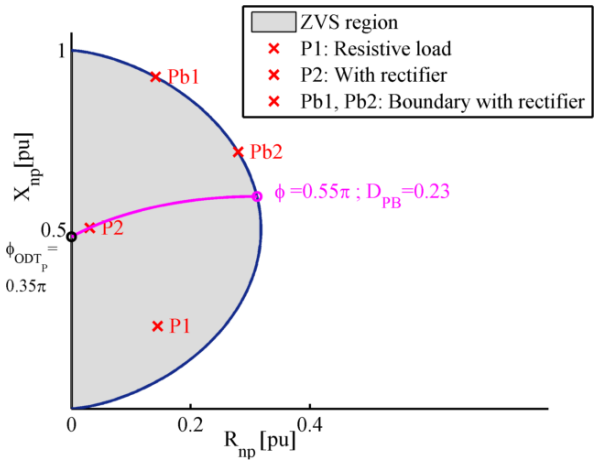
(c) An operating point ($P_{1,B}$) located in the boundary of NELIP plane with $V_{in} = 4V$, frequency= $106kHz$, $V_o = 5V$. C1: Gate voltage of the S1; C2: Gate voltage of the S2; C3:Inverter's switching voltage v_{FP}.



(d) An operating point ($P_{2,B}$) located in the boundary of NELIP plane with $V_{in} = 4V$, frequency= $169kHz$, $V_o = 5V$. C1: Gate voltage of the S1; C2: Gate voltage of the S2; C3:Inverter's switching voltage v_{FP}.

TABLE I: Measuring the resonant current's phase ϕ, and $\phi_{ODT,P}$.

Point	ϕ (rad)	$\phi_{ODT,P}$ (rad)
P_1	0.37π	0.26π
P_2	0.54π	0.37π



(e) Map of operating points in the inverter's NELIP.

Fig. 10: Experimental results.

IV. ZVS REGION FOR THE RECTIFIER NETWORK

A. ZVS boundary of active rectifier network

In critical points located on the boundary of the ZVS region, the resonant current crosses zero precisely when the voltage across C_{out} reaches its peak value at the end of DT. This further means $\Delta\phi_s = 0$ or $\phi_{IS} = \phi$ in waveforms shown in Fig. 5, where generally the relationship between the phases is $\phi_{IS} = \phi + \Delta\phi_s$. Substituting $\Delta\phi_s = 0$ into Equations (6−8) results in:

$$R_{ns} = \frac{8R_{Ln}}{(2\pi + R_{Ln})^2} \tag{22}$$

and the effective reactance is described as

$$X_{ns} = \sqrt{\frac{8R_{Ln}}{\pi}}\frac{2\pi - R_{Ln}}{(2\pi + R_{Ln})^2} - \frac{1}{\pi}\phi_{ODT,S} \tag{23}$$

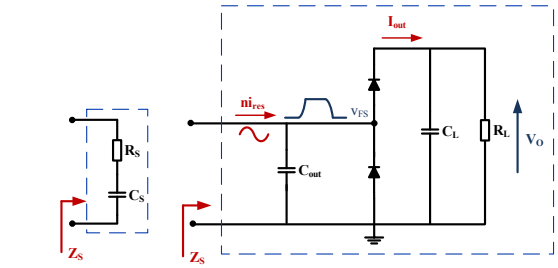
where

$$\phi_{ODT,S} = cos^{-1}\left(\frac{2\pi - R_{Ln}}{2\pi + R_{Ln}}\right) \tag{24}$$

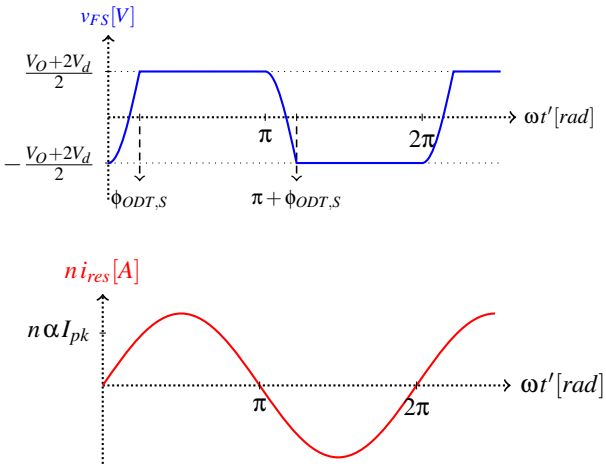
If $C_{out} = 2C_d$ the results are in good agreement with previous research [36].

B. Diode rectifier network

The analysis for passive rectifier network is the same as in Subsection IV-A, after substituting $\Delta\phi_S = 0$. When the resonant current passes through zero from negative direction to the positive direction, it starts to charge the output capacitance until the voltage across C_{out} reaches a voltage slightly higher than the output voltage to the value of V_d, which causes the high-side diode to start to conduct. Then, the switching voltage v_{FS} is clamped to the positive rail voltage until the resonant current changes direction from the positive to negative. Therefore, the output capacitance starts to discharge until the v_{FS} reaches the negative rail. In this situation, the resonant current does not necessarily crosses zero at the end of DT, which makes it different to the case described in Subsection IV-A. Furthermore, the voltage drop across the diodes affects the

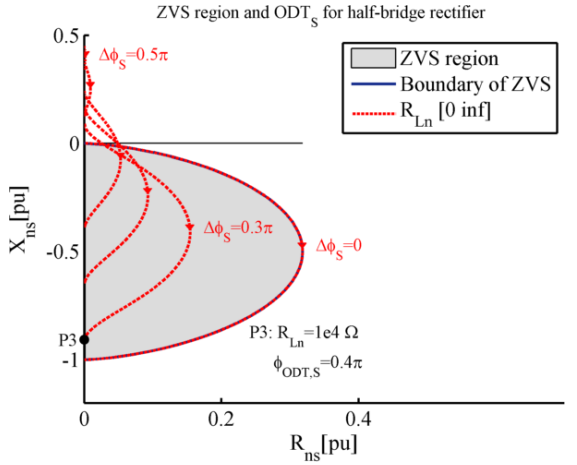


(a) Elecreical equivalent circuit.

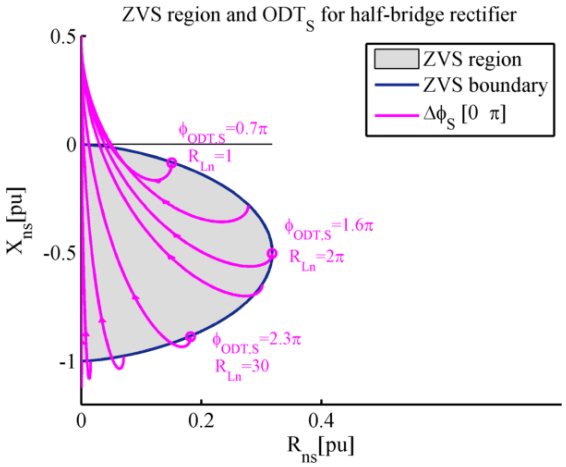


(b) Signal waveforms i_{res} and v_{FP}.

Fig. 11: Half-bridge rectifier in the secondary side of the piezo transformer, forward voltage conduction of the diode V_d are considered. Passive rectifier network and signal waveforms for diodes $\Delta\phi_s = 0$ are shown.



(a) Map of points with different phase shift in the full range of the load.



(b) Map of points with different normalized load values.

Fig. 12: ZVS region for the rectifier network.

impedance seen from the input of the rectifier. While the rectifiers are conducting, the output voltage of the PT is clamped to the output voltage, which is considered as a DC voltage V_o. Thereby, the output current goes through the load resistance.

$$V_o = R_L < I_{out} >= \frac{2nR_L I_{pk}}{2\pi + R'_{Ln}} \tag{25}$$

where $R'_{Ln} = R_{Ln}(1+2V_{df})$ and $V_{df} = \frac{V_d}{V_o}$, which results in

$$P_{out} = V_o < I_{out} >= \frac{4}{R_L}\left(\frac{nI_{pk}}{2\pi + R'_{Ln}}\right)^2 \tag{26}$$

The effective impedance Z_{ns} is found by the same equations as in Section IV-A, where the normalized load resistance will be R'_{Ln} by considering the forward voltages of the diodes.

$$R_{ns} = \frac{8R'_{Ln}}{(2\pi + R'_{Ln})^2} \tag{27}$$

and

$$X_{ns} = \sqrt{\frac{8R'_{Ln}}{\pi}}\frac{2\pi - R'_{Ln}}{(2\pi + R'_{Ln})^2} - \frac{\phi_{ODT,S}}{\pi} \tag{28}$$

$$\phi_{ODT,S} = cos^{-1}\left(\frac{2\pi - R'_{Ln}}{2\pi + R'_{Ln}}\right) \tag{29}$$

These equations are in agreement with previous research [18].

C. Rectifier's results

Fig. 12 shows the rectifier's ZVS region and its boundary in the NELIP plane. The subfigure at the bottom of the figure shows curves when the R_L is fixed to one value and the locus of points with different $\Delta\phi_s$. For instance, if the load resistance is $R_{Ln} = 2\pi$, the phase related to the optimum DT can be in the range of $\phi_{ODT,S} = [1.5\pi, 1.6\pi]$ for the points inside the ZVS region. The subfigure on the top of the figure shows the locus of points with different load resistance where $\Delta\phi_{ODT,S}$ is fixed to a certain value and the normalized load varies. The point P_3 is located on the curve where $\Delta\phi_S = 0.3\pi$, $R_{Ln} = 10k\Omega$, and $\phi_{ODT,S} = 0.4\pi$. Experimental results are shown in Fig. 13, for PT-based converters with resistive load and half-bridge rectifier. In each case, two operating points are considered where the inverter's switches have soft switching and hard switching. The related parameters for these four operating points are measured and mapped to the inverter's NELIP plane in Fig. 14. The experimets show matched results with the analysis. Results in Figs. 12 and 13 show that operating points

for which ZVS is obtained are located inside the ZVS region and the operating points for which ZVS is not attained (hard switching), are located outside the ZVS region.

D. ZVS region of the converter

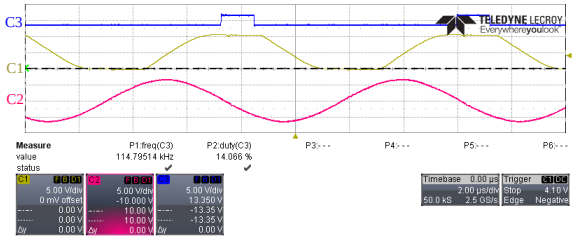
Fig. 15 shows the equivalent circuit seen from the primary side of the converter, where $C_{Pe} = CC_s/(n^2C + C_s)$ and $R_{Pe} = R + n^2 R_s$. Therefore,

$$Z_{Pe} = R_{Pe} + X_{Pe} = R_{Pe} + j\left(\omega L - \frac{1}{\omega C_{Pe}}\right) \qquad (30)$$

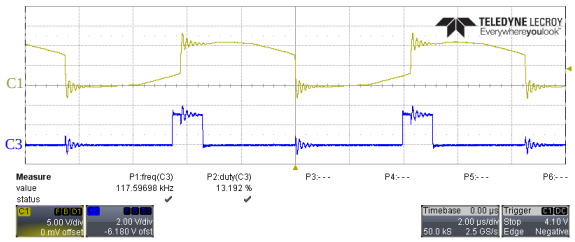
The Z_{Pe} can be mapped into the NELIP to show whether or not the ZVS can be attained. In order to find R_{Pe} the topology of the converter should be considered. Furthermore, the operating frequency of the converter has a significant effect on the mapped ZVS region, which is from the rectifier to the inverter NELIP plane. This method is used to define the common area between the two ZVS regions. The overlapping area shows that soft switching can be obtained for the inverter's and rectifier's switches (related to v_{FP} and v_{FS}) for the operating points located inside this particular area. In some other areas, the ZVS region can be obtained for either v_{FS} or v_{FP} or non of them. Fig. 16a shows the mapped ZVS region of the rectifier to the inverter's NELIP plane. The rectifier's ZVS region is mapped to the primary-side of the converter for two different frequencies, f_{res} and $1.02f_{res}$, where f_{res} is the transformer's resonant frequency utilized in all the experiments. It shows that the overlapping region where ZVS can be obtained for both the inverter and the rectifier network varies in terms of operating frequency, which is expected. Fig. 16b shows the ZVS regions for the operating point P_2 demonstrated in Fig. 10 for which the switching frequency is $114.8\,kHz$. The point P_2 is situated inside the common area of the ZVS regions and it is shown in Fig. 10.The Flowchart shown in Fig. 17 shows a simple step by step design procedure for obtaining ZVS for all switches based on the presented analysis. This suggested design procedure is applicable for the cases where there is access to measure or detect the resonant current's amplitude and phase.

V. Conclusion

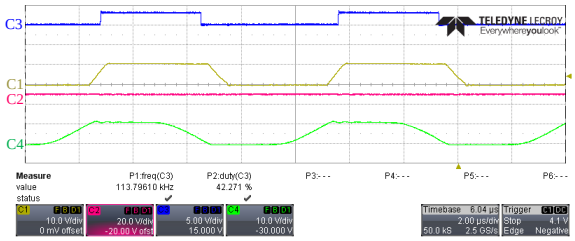
This paper has proposed a new method of analysis to find ZVS regions for the inverter and the rectifier networks inside the PT-based SMPS. Comprehensive equations were provided for the first time and were proven by simulation and experimental results. Experiments showed mapped operating points for inductorless PT-based converters in the NELIP plane. Furthermore, this analysis estimates the possibility of ZVS achievement and optimum DT for different operating points in terms of load variations both for the inverter and the rectifier networks. In practice providing a condition for attaining ZVS in all switches is a challenging task. Therefore, the work has further presented guidelines to find the region where all the converter's switches have soft switching. The proposed method is generally applicable for any type of resonant converter, but details are described for inductorless PT-based converters.



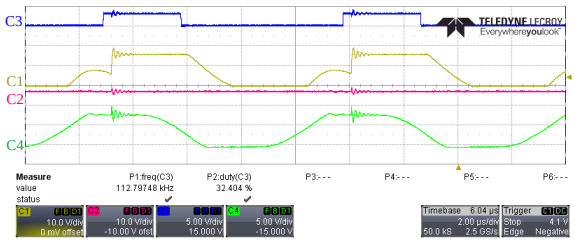
(a) Converter with resistive load and soft switching, related to the point P_7 in Fig. 14. $f_{res} = 114.8kHz$. C_1: The switching voltage v_{FP}; C_2: Resonant current; C_3: The gate voltage of S1.



(b) Converter with resistive load and hard switching, related to the point P_6 in Fig. 14. $f_{res} = 117.6kHz$. C_1: The switching voltage v_{FP}; C_3: The gate voltage of S1.



(c) Converter with rectifier network and soft switching, related to the point P_5 in Fig. 14. $f_{res} = 113.8kHz$. C_1: The switching voltage v_{FP}; C2: The output voltage $V_o = 10\ V$; C_3: The gate voltage of S1; C_4: The switching voltage v_{FS}.



(d) Converter with rectifier network and hard switching, related to the point P_4 in Fig. 14. $f_{res} = 112.8kHz$. C_1: The switching voltage v_{FP}; C_2: The output voltage $V_o = 10\ V$; C_3: The gate voltage of S1; C_4: The switching voltage v_{FS}.

Fig. 13: Four operating points for PT-based converter; (a): converter has resistive load attained soft switching; (b): converter has resistive load with hard switching; (c): converter has rectifier network attained soft switching; (d): converter has rectifier network with hard switching.

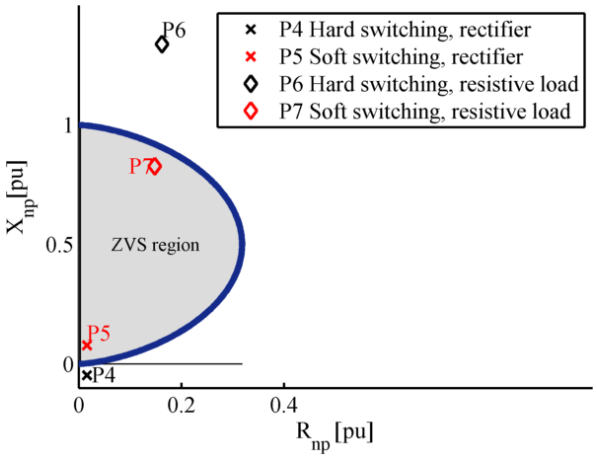


Fig. 14: Mapping of the four operating points shown in Fig. 13.

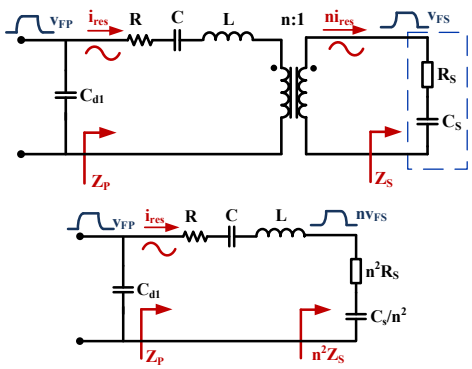
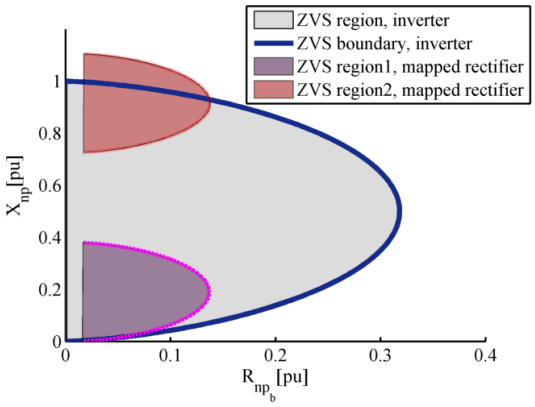
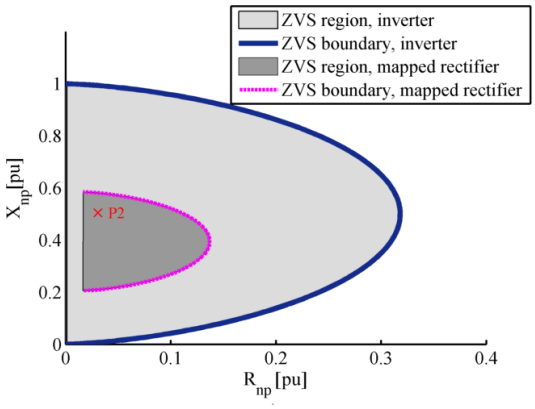


Fig. 15: Equivalent impedances of the converter seen from the inverter.



(a) The mapped rectifier's ZVS region for different switching frequencies.



(b) The mapped rectifier's ZVS region for the switching frequency of 114.8kHz.

Fig. 16: ZVS regions of the rectifier and the inverter seen from the inverter's side.

VI. Appendix

A. Deriving Z_{ns} for the rectifier

During the dead time period when the resonant current is positive and charges the output capacitor from the negative rail to the positive rail, v_{FS} is described as:

$$v_{FS}(t') = v_{FS}(0^-) + \frac{1}{C_{out}} \int_{\Delta\phi_s}^{\omega t'} n I_{res}(t)\, d\omega t' \tag{31}$$

The voltage across the output capacitor reaches the positive rail $v_{FS} = \frac{V_0}{2}$ at $\omega t' = \Delta\phi_s + \phi_{ODT,S}$. Thereby, V_o is found as:

$$V_0 = \frac{n I_{pk}}{\omega C_{out}} \left(cos(\Delta\phi_s) - cos(\Delta\phi_s + \phi_{ODT,S})\right) \tag{32}$$

The resonant current goes to the output in the period that high-side switch, $S3$, is on, and the average of the current appears to the output:

$$< I_{out} > = \frac{n I_{pk}}{2\pi} \left[cos(\Delta\phi_s + \phi_{ODT,S}) + cos(\Delta\phi_s)\right] \tag{33}$$

the output voltage is constant; therefor, the output current goes through the load resistance $V_o = R_L < I_{out} >$, which yields:

$$cos(\Delta\phi_s + \phi_{ODT,S}) = \frac{2\pi - R_{Ln}}{2\pi + R_{Ln}}\, cos(\Delta\phi_s) \tag{34}$$

where $R_{Ln} = \omega R_L C_{out}$ is a normalized load resistance. Substituting Equation (34) into Equations (33) and (32) results in:

$$< I_{out} > = \frac{2 n I_{pk}\, cos(\Delta\phi_s)}{2\pi + R_{Ln}} \tag{35}$$

The equivalent resistor and capacitor are found as

$$R_s = \frac{8 R_L \cos^2(\Delta\phi_s)}{(2\pi + R_{Ln})^2} \tag{36}$$

$$C_s = \frac{\pi C_{\text{out}} (2\pi + R_{Ln})^2}{cos(\Delta\phi_s)(2\pi - R_{Ln})A + (2\pi + R_{Ln})^2 (\phi_{ODT,S} + sin(2\Delta\phi_s))} \tag{37a}$$

$$A = (2\pi + R_{Ln}) \sqrt{1 - \left(\frac{2\pi - R_{Ln}}{2\pi + R_{Ln}}\right)^2 cos^2(\Delta\phi_s)} \tag{37b}$$

$$\phi_{ODT,S} = cos^{-1}\left(\frac{2\pi - R_{Ln}}{2\pi + R_{Ln}}\right) cos(\Delta\phi_s) - \Delta\phi_s \tag{37c}$$

This then yields the normalized impedances $Z_{ns} = R_{ns} + jX_{ns}$ by multiplying ωC_{out} with the R_S and X_S

$$Z_{ns} = \omega C_{out} Z_S = R_{ns} + jX_{ns} \tag{38}$$

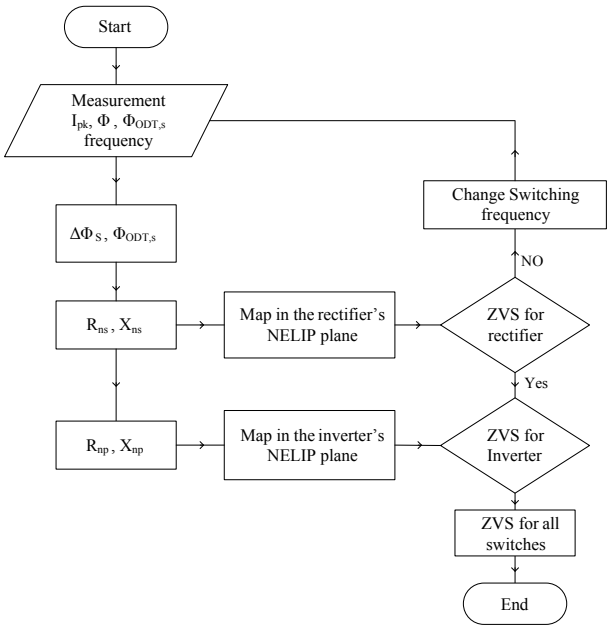


Fig. 17: A step by step design method applicable where there is access to dynamically measure the resonant current.

Note that R_S and C_S depends on R_{Ln} where R_{Ln} depends on ω and load resistance R_L.

B. Deriving Z_{np} for the inverter

Fig. 6 shows waveforms of the voltage v_{FP} and the resonant current i_{res}. In the time slot, $0 \leq \omega t \leq \omega t_{ODT,P}$; $i_{C_{in}} = -i_{res}$, then v_{FP} is found as

$$v_{FP}(t) = \frac{I_{pk}}{\omega C_{in}}\, cos(\omega t - \phi) - cos(\phi)) - \frac{V_{DC}}{2} \tag{39}$$

At $\omega t = \phi_{ODT,P}$, the switching voltage reaches the positive rail. Therefore, $v_{FP}(\phi_{ODT,P}) = \frac{V_{DC}}{2}$, which yields

$$v_{FP} = \frac{V_{DC}}{2} = \frac{I_{pk}}{\omega C_{in}}\, cos(\omega t - \phi) - cos(\phi)) - \frac{V_{DC}}{2}$$

Solving above equation for I_{pk} gives

$$I_{pk} = \frac{V_{DC}\,\omega C_{in}}{cos(\phi_{ODT,P} - \phi) - cos(\phi)} \tag{40}$$

Substituting Equation (40) into Equations (9) and (39) results in a general equation of i_{res} and v_{FP}:

$$i_{res}(t) = \left(\frac{V_{DC}\,\omega C_{in}}{cos(\phi_{ODT,P} - \phi) - cos(\phi)}\right) sin(\omega t - \phi)\; 0 \leq \omega t \leq 2\pi$$

$$v_{FP}(t) = \frac{V_{DC}}{2[\, cos(\phi_{ODT,P} - \phi) - cos(\phi)\,]} \qquad 0 \leqslant \omega t \leqslant \phi_{ODT,P}$$
$$[\, 2cos(\omega t - \phi) - cos(\phi_{ODT,P} - \phi) - cos(\phi)\,] \tag{41}$$

The fundamental components of $v_{FP}(t)$ and $i_{res}(t)$ can be found by Fourier analysis. The corresponding phasor representation of $v_{FP}(t)$ for the fundamental component of the Fourier series is

$$(\overline{V}_{FP})_1 = \frac{1}{\pi}\frac{V_{DC}}{[\, cos(\phi_{ODT,P} - \phi) - cos(\phi)\,]} \qquad 0 \leqslant \omega t \leqslant 2\pi$$
$$[\, \frac{-1}{2} sin(2\phi_{ODT,P} - \phi) - \frac{1}{2} sin(\phi)$$
$$+ \phi_{ODT,P}\,(cos(\phi) - j\, sin(\phi))$$
$$\frac{1}{2}\, j\, cos(2\phi_{ODT,P} - \phi) + \frac{1}{2}\, j\, cos(\phi)\,] \tag{42}$$

Therefore, the fundamental component of the resonant current is represented by the phasor

$$(\overline{I}_{res})_1 = \frac{-V_{DC}\,\omega C_{in}}{cos(\phi_{ODT,P} - \phi) - cos(\phi)}\,[\, sin(\phi) + j\, cos(\phi)] \qquad 0 \leqslant \omega t \leqslant 2\pi \tag{43}$$

The effective equivalent impedance seen by the switching network is $Z_P = (\overline{V}_{FP})_1/(\overline{I}_{res})_1 = R_P + jX_P$. Normalizing Z_P by multiplying by ωC_{in} results in Z_{np} as below.

$$Z_{np} = \omega C_{in} Z_P = \omega\, C_{in}\, \frac{\overline{V}_F}{\overline{I}_{res}} = R_{np} + jX_{np} \tag{44}$$

ACKNOWLEDGMENT

The authors would like to thank Noliac A/S for supplying prototype of piezoelectric transformers as well as "The Danish National Advanced Technology Foundation" for their financial support.

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Appendix I

Optimum phase in the self-oscillating loop for piezoelectric transformer-based power converters

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Under review at

IEEE Transaction on Power Electronics, IEEE-TPEL (2016)

Optimum phase in the self-oscillating loop for piezoelectric transformer-based power converters

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***Abstract*—A new method is implemented in designing of self-oscillating loop for driving piezoelectric transformers. This method can also be used for other types of converters, e.g. resonant converters. The implemented method is based on combining both analog and digital control systems. Digitized time delay, or in other words digitized phase shift through the self-oscillating loop results in very precise frequency control and ensures optimum operation of the piezoelectric transformer in terms of gain and efficiency. In this work, additional time delay is implemented digitally for the first time through a 16 bit digital-to-analog converter in the self-oscillating loop. Delay control setpoints updates at a rate of 417 kHz. The new design of the optimum delay circuit provides 1ns time resolution for the control in the self-oscillating loop. This allows the control loop to dynamically follow frequency changes of the transformer in each resonant cycle. Ultimately, by selecting the optimum phase shift, maximum efficiency under the load, and temperature condition is achievable. In this work efficiency improvement of 9% in the experiments is achieved. The operation principle behind self-oscillating is also discussed in this paper.**

***Index Terms*—Optimum delay line; self-oscillating loop; phase shift; switch mode power supply; zero-voltage switching; piezoelectric transformer.**

NOMENCLATURE

ADL-CEZC	Adjustable delay line circuit added to the CEZC block.
C	Resonant capacitance of the piezoelectric transformer.
C_{d1}	Input electrode capacitance of the piezoelectric transformer.
C_{d2}	Output electrode capacitance of the piezoelectric transformer.
CEZC	Current estimation zero crossing.
DDL	Dynamic delay line.
DDL_{in}	Input signal of the DDL block.
DDL_{out}	Output signal of the DDl block.
EDDL_{in}	Input signal of the digitized delay line block passed through the edge detector.
FF	Flip-flop.
FPGA	Field-programmable gate array.
FTD	Fixed time delay.
HS	High-side gate voltage.
i_{res}	The resonant current of the piezoelectric transformer.
L	Internal inductance of the piezoelectric transformer.
LS	Ligh-side gate voltage.
MOSFET	Metal-oxide-semiconductor field-effect transistor.
ODL	Optimum delay line circuit block.
ODL_{out}	Output signal of the optimum delay line circuit block.
R	Dielectric losses inside the transformer.
R_m	Matched load for the piezoelectric transformer.
v_F	Switching voltage.
$\text{ZC}i_{res}$	Zero crossed signal of the estimated resonant current.
ZVS	Zero-voltage switching.
ω	Switching angular frequency.
ϕ_I	Phase shift of the resonant current with reference to the turn-off time of the low-side switch.

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I. INTRODUCTION

Piezoelectric transformers' (PT) voltage gain, resonance frequency and efficiency change with variation of their load and temperature [1]–[4]. Therefore, in order to operate a PT in its optimum point, located slightly above the resonant frequency [5], it is necessary to follow changes in the resonance frequency [1], [6]–[8].

When the inductorless topology is employed for the PT-based converters, the operating frequency of the PT is reduced to a narrow band in which PT shows an inductive behavior. Therefore, a very small variations in the resonant frequency can easily cause instability in the converter. However, keeping operating frequency in a proper point which is slightly above resonant frequency is hard to be attained by open loop. As a consequence, closed loop control is indispensable for compensating influence of parameters such as frequency and temperature, in order to have stable operation of PT and consequently accurate performance of the converter [9]–[13].

The options for the closed-loop are phased locked loop (PLL) and self-oscillating loop control methods. The PLL approach which is also a controlled oscillator is not a good option for the inductorless PT-based converters [5]. Therefore, the self-oscillating loop is used for the closed-loop control of the PT's operating point.

The self-oscillating loop is able to adjust its phase shift to follow the PT's resonant frequency. Therefore, implemented

adjustable phase shift compensates for the rest of the phase shift in the loop for frequency variations. This is more important when a PT-based converter is operating in bi-directional mode for energy recovery [10]. As an example, when the energy transfered by the converter needs to be controlled to maintain DC output voltage at different voltage levels, the PT's load changes [8], [10]. Any changes in the PT's load causes a change in its operating point [8]. In order to keep the PT operating at its most efficient point, its operating frequency should be changed. This is performed by changing the converter's switching frequency. The switching frequency is controlled through a self-oscillating loop [9], [14]. Therefore, by changing the predesigned phase shift, the switching frequency follows variations in the PT's resonant current.

Phase shift compensation with high resolution becomes necessary especially when the load of the converter is variable. Notably, the PT's transfer function also differs by temperature rise [1], [15]. These variations directly translates to PT's load variations. If the total phase shift of the loop is not properly adjusted to an integer factor of 360°, it causes a damping of the resonant current. Therefore, closed-loop operation cannot be achieved and basically the converter will not start working. Thereby, very fine resolution for phase shift adjustment is required. A more thorough explanation of the self-oscillating loop is provided in the Section II.

Several attempts have done for closing the feedback loop in the PT-based switch-mode power supply (SMPS) [9], [11], [12], [16]. In previous research, an adjustable time delay block that controls the total loop phase has been implemented for a bi-directional converter through an analog circuit. This was done by detecting peaks in the PT's resonant current [10], [17]. In the closed-loop operation, 360° phase difference cannot be ensured for the load or temperature variations of the PT, particularly in bi-directional operation [10]. The principle behind self-oscillation obtained in the prior art is explained in the Sub-section II-A and experimental results are provided inthe Sub-section II-C.

The analog implementation becomes unstable when approaching 0° in the real implementation [10]. To solve this problem, a digitalized phase shift compensation is applied in this paper. Changes in the PT's resonant frequency are compensated for the closed-loop by detecting and adding required phase shift in order to obtain a full loop phase shift of 360°. Furthermore, digital implementation allows for fine changes in time delay inside the loop for frequency tracking. Compensation is performed by adding a finely-controlled time delay to the feedback chain. Resolution of the applied time delay is 1 ns. This ensures that the added time delay is finely controllable in order to precisely adapt the frequency of the self-oscillating loop and match changes in the PT's operating point. More explanation about the proposed method is provided in the Sub-section III-A and experimental results are provided in the Sub-sections II-C and IV. This further ensures soft switching operation of the PT and therefore, the highest efficiency attainable.

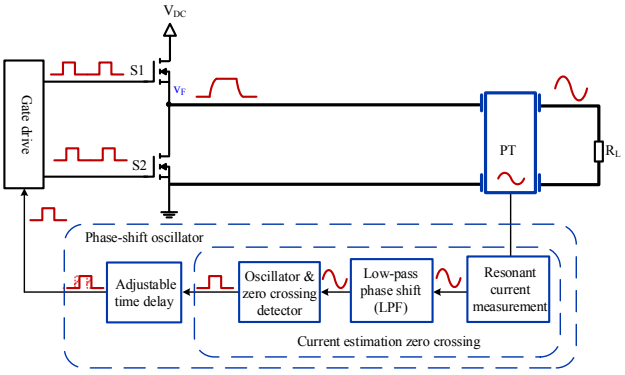


Fig. 1: Block diagram of prior art self-oscillating loop.

II. Self-oscillating loop for PT-based converters

A. Principle and design considerations

Essentially, two requirements need to be satisfied in order to produce sustained oscillation in closed-loop. One is that phase angle of the entire loop should be an integer multiple of 360°; the other requirement is that the loop gain should be greater than unity to start-up oscillation. The former condition is fulfilled by adjusting phase shift through the loop. The latter condition is fulfilled by designing through a comparator since the comparator's gain can be considered infinite and therefore its input becomes saturated to the rail voltages, generating square waves in the output. In the designed circuit there is a hysteresis controller which operates as an oscillator during start-up with a frequency close to or lower than the PT's resonance frequency. The frequency of square waves can be designed to be slightly lower than the resonance frequency. In this case, it is ensured that oscillation does not lock into the second or higher resonance frequencies of the PT. Furthermore, it is close to the PT's fundamental resonance frequency and this helps minimizing time for the loop to be locked. Fig. 1 shows the block diagram for the self-oscillating loop [9], and Fig. 2 shows the circuit for the self-oscillating loop together with the PT-based power stage with matched load. Equation (1) represents the time period of this self-induced oscillation.

$$T = R'_F C_3 \, ln(1 + \frac{2R_4}{R_5}) \tag{1}$$

where R'_F is equivalent resistance of two parallel resistors, R_F and R_3. The resistor R_5 is used in order to provide an initial condition for the capacitor and helps with oscillation start-up. The ratio of R_4/R_5 forms the hysteresis window to specify a voltage range and to build the appropriate level of noise immunity.

Thereby, small perturbations in the loop start the self-induced oscillation. This results in self-excitation of the resonant current inside the PT during the start-up. Self-excited square waves with a frequency lower than or close to the resonant frequency of the PT will excite resonant modes inside the transformer. This is achieved by the fundamental frequency of the square waves and its higher order harmonics. Since the PT is operating as a high Q band-pass filter (BPF), it filters

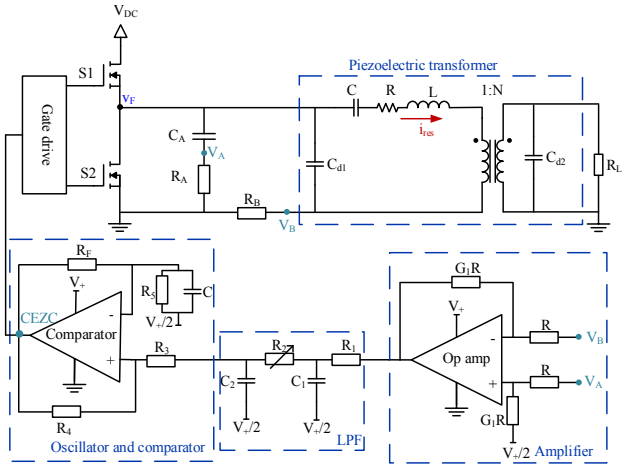


Fig. 2: Circuit design demonstrates principle of self-oscillating loop in PT-based SMPS.

higher order harmonics out and transfers the fundamental component to its output. The electrical quality factor of the PT is derived as:

$$Q = \frac{1}{\omega C_{d2} R_L} \tag{2}$$

where $\omega = 1/\sqrt{LC}$ is the series-resonance angular frequency of the PT [18], [19]. Therefore, resonant current is considered as sinusoidal waveform described in (3).

$$i_{res}(t) = I_{pk}(t)\, sin(\omega t - \phi_I) \tag{3}$$

where $\phi_I \in [0, \pi]$ is the current phase angle.

The amplitude of the fundamental resonant current grows with time, until its level is large enough compared to the self-induced oscillator. Since the amplitude of the sinusoidal waveform at the output of low-pass filter (LPF), shown in Fig. 1, is greater than the amplitude of the self-induced oscillation waveform, the oscillator operates as a comparator. This allows the comparator's behavior to change from that of an oscillator to that of a true comparator. Therefore, it compares resonant current with a DC level in order to mark the zero crossing of the current. The loop is designed for the case where the PT is connected to the resistive matched load [9] by considering Mason's equivalent parameters [20], [21].

$$R_{matched} = \frac{1}{\omega C_{d2}} \tag{4}$$

The reasoning behind this design choice is that a matched load is considered to be the worst-case scenario for a PT, in terms of achieving soft switching [22]. Zero-voltage switching (ZVS) is a form of soft switching considered in this work. Fig. 3 shows the trend of load resistance versus ZVS factor [22]. At the matched load, the energy transfer through the PT is maximum and therefore its efficiency is maximized as well. This results in a point of minima on the ZVS factor axis [8], [21]. The role of the ZVS factor is to provide the worst-case scenario for analyzing PTs in terms of soft switching capability. Therefore, if ZVS is achieved for the matched load, it will be obtained for other loads as well [22]. The worst-case

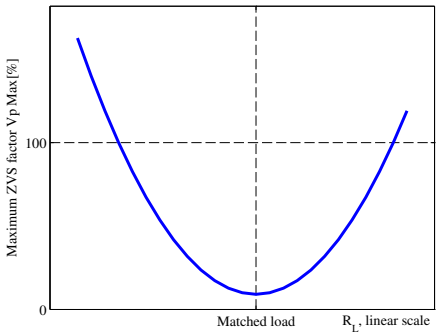


Fig. 3: Soft switching factor for PT as a function of load resistance.

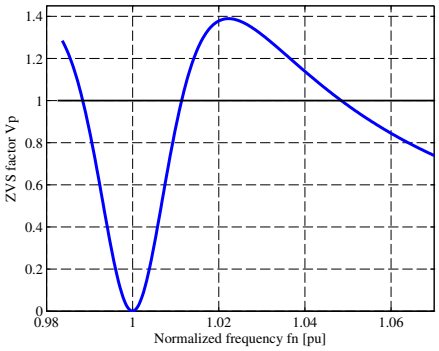


Fig. 4: Normalized frequency vs. normalized soft switching factor for PT; $R = 98\ m\Omega$, $C = 11.27\ nF$, $L = 733$ µH, $C_{d1} = 112\ nF$, $C_{d2} = 14.6\ pF$, $N = 112$.

explanation of approximated ZVS factor is expressed based on empiric analysis of ZVS in the following equation [23]:

$$V_p' = (0.304\ \frac{1}{n^2}\frac{C_{d2}}{C_{d1}} + 0.538) \cdot (0.585\eta + 0.414) \tag{5}$$

where η is the efficiency of the transformer. V_p' is ZVS factor and should be roughly above 1 in order to obtain soft switching. Therefore, the ZVS region is a narrow frequency range above the resonance frequency, where the PT behaves as an inductor and $V_p' > 1$. Furthermore, the ZVS bandwidth of the PT is a ratio of L/C for a constant resonance frequency [22]. Equation (5) and Fig. 4 are based on a primary analysis of ZVS in order to justify the necessity to design a driver and self-oscillating loop for the matched load, where Fig. 4 shows the soft switching factor for a PT as an example [22].

B. Current estimation zero crossing (CEZC)

The resonance current in the PT is reconstructed within two time intervals. Voltage V_B across R_B shown in Fig. 2 measures this resonance current while the switches are on. Voltage V_A across R_A measures the resonant current during dead time, while both switches are off. The resonance current in this period is supplied by the PT's input capacitor C_{d1}. Therefore, the current passing through C_{d1} follows the resonant current and can be measured by differentiating the voltage across C_{d1}. This is performed by using C_A and R_A as a differentiator. C_A should be approximately 10 times lower than C_{d1} in order not to affect the input capacitance of the PT and, subsequently,

TABLE I: PT EQUIVALENT PARAMETERS

Parameter	Value	Parameter	Value
C_{d1}	3.83 nF	C_{d2}	626 pF
C	565 nF	R	5.63Ω
L	3.5 mH	N	3.57

TABLE II: Phase shift during one switching cycle in the self-oscillating loop; switching frequency is 118.3 kHz with time period of 8.45µs.

Delay	Time[µs]	Phase[°]	Duty cycle%
HS→HSGD	1.59	67.8	18.85
HSGD→I_{est}	0.27	11.5	3.19
I_{est}→LPF	6.09	259.4	72.04
LPF→CEZC	0.5	21.3	5.92
Total	8.45	360	100

dead time and ZVS factor of the transformer. R_A and R_B are also chosen to have low values and in order to set a ratio between V_A and V_B for the input of the op-amp. By subtraction of these two voltage waveforms through the op-amp, an approximate sine waveform representing the resonant current will be reconstructed in the output [5], [9], [24]. Fig. 2 shows the voltages V_A and V_B. Therefore, voltage in the output of the op-amp is:

$$V_{out}|_{opamp} = G_1(V_A - V_B) = G_1(R_A C_A \frac{d}{dt} V_{C_{d1}} - R_B \overbrace{i_{res}|_{sw:off}}) \quad (6)$$

The estimated current has a 180° phase shift compared to the resonance current which results in the same zero-crossing points. Thereafter, the estimated resonance current is transmitted to a second order low-pass filter (LPF) which provides an additional phase shift through the feedback loop. In order to have adequate phase shift through the LPF, its cut-off frequency is adjusted to be around the resonance frequency. Furthermore, some harmonics are eliminated by the LPF, resulting in a smoother waveform which contains the fundamental harmonic of the resonance current. The filtered signal is transmitted to the comparator and generates a square wave indicating the zero crossing of the input signal. The square wave signal is fed into the adjustable time delay in order to compensate for the rest of the phase shift to have a total of 360° in the whole loop from the input of the gate driver to the output of feedback loop. In case the switching frequency needs to be decreased, the total phase shift should be increased.

C. Experimental results

Fig. 5 shows experimental waveforms. The designed board is shown in Fig. 6. A radial mode PT with Mason's equivalent circuit, shown in Fig. 2, is used, driven by square wave signals with a switching frequency of 118.3 kHz, while driving a resistive load of 300 Ω. Moreover, reconstructed resonant current from voltages V_A and V_A is shown in Fig. 5. Furthermore, the equivalent parameter values of the PT are measured and shown in Table I. Phase shifts and corresponding time delays between stages are measured and shown in Table II.

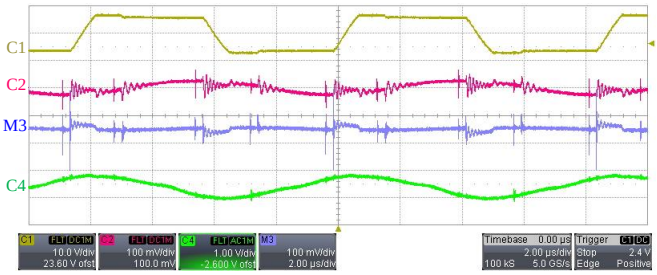


Fig. 5: Reconstruction of the resonant current. C1: switching voltage v_F, C2: V_A, M3: V_A, C4: G1 (V_A-V_B).

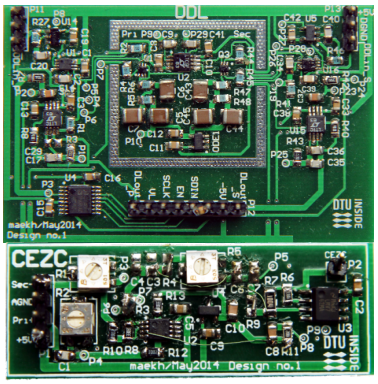


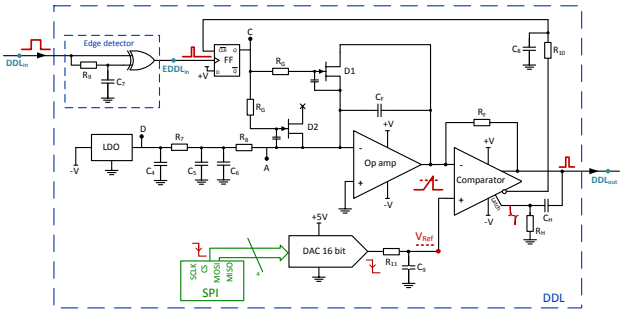
Fig. 6: ODL and CEZC-A boards.

III. Phase-Shift Self-Oscillating Loop with Optimum Delay Line

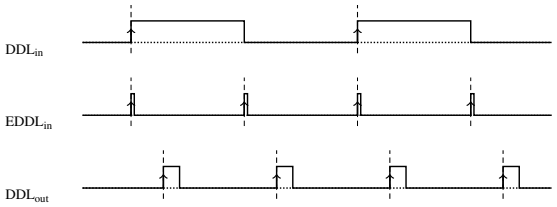
A. Digitized delay line (DDL)

Initial investigation of the time step resolution which required finely adjustment of the total phase shift in the loop. This investigation was performed by mapping relative changes in the frequency to the output voltage variations. The result of this investigation shows that there is an measurable change in the amplitude of the PT's output voltage for every 10 Hz change in switching frequency. For example, if the operating frequency of 100 kHz increases by 10 Hz, the output voltage shows a considerable change in the amplitude e.g. 6 V. This output voltage variation depends on the transformer and the range of the operating frequency. Therefore, a precision of minimum 10 Hz in the frequency is required for dynamic time delay which is equivalent to 1ns time delay resolution. Thereby, a phase shift self-oscillating closed loop is designed together with the contribution of the digital-to-analog converter (DAC) and field-programmable gate array (FPGA). These are used to implement a high-resolution time delay inside the dynamic time delay block.

Fig. 7 shows the circuit designed for the dynamic time delay (DDL) together with the drawing of the input and output waveforms of the DDL circuit block. In this block, the input signal (DDL_{in}) is first transformed into edge-detecting one-shot pulses ($EDDL_{in}$) which are then used as a clock source for the flip-flop (FF). The signal froms this FF is then used to reset the hardware integrator present in the



a: Digitized time delay circuit (DDL).



b: The input and output signals of the DDL block shows an arbitrary delay with 1 ns step resolution.

Fig. 7: DDL circuit and input and output signals.

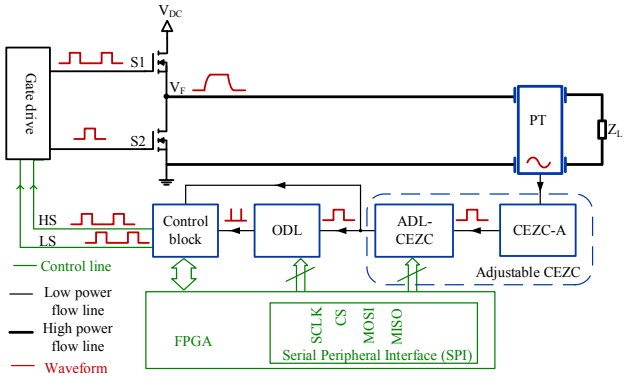


Fig. 8: Block digram of self-oscillating loop with optimum phase.

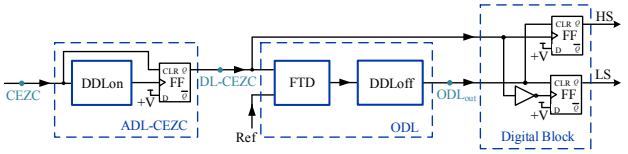
circuit. Namely, when the input signal edge-triggers the FF, the feedback capacitor in the op-amp feedback starts charging, thereby creating a fixed voltage slope. This is then compared to the variable reference voltage provided by the DAC. Thereafter, the complementary output of the comparator resets the FF which consequently turns the metal-oxide-semiconductor field-effect transistor (MOSFET) D1 on and discharges the feedback capacitor, thereby resetting the integrator. Since the input pulse triggers the start of the integration, the variable reference provided to the comparator by the DAC coupled with the voltage slope work together to create a time-delayed version of the input pulse which is proportional to the DAC output value. The output of the comparator is then latched for a short time by its own output through a high-passed signal to its latch pin, resulting in one-shot pulses at the output of the DDL (DDL_{out}).

B. Self-oscillating loop based on the optimum time delay

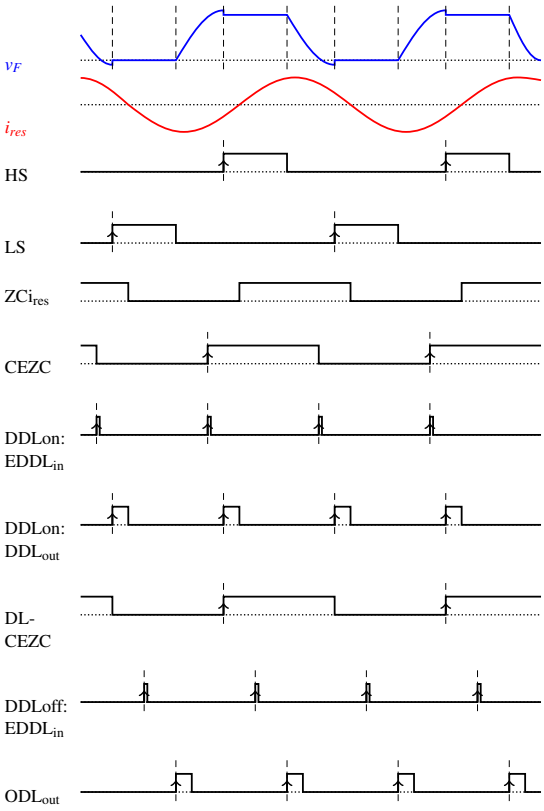
A new phase shift self-oscillating loop for the PT-based converter is designed and proposed with the combination of the analog and digital designs. Fig. 8 shows the simplified block diagram of the proposed closed-loop with main blocks. The output signal of the current estimation zero-crossing (CEZC) block is a 50% duty cycle square wave signal, having the same frequency as the PT. For the closed-loop operation the reference signal is considered as high-side gate voltage (HS). For tracking the PT's frequency the reference is considered as the output of the CEZC block. In this design rising edge of the CEZC is used for turning on the high-side switch. By working on the different operating frequency ranges, there is need to adjust the phase shift of the LPF inside the CEZC analog block to synchronize the CEZC and HS signals. In order to avoid adjusting phase shift in the hardware, a digital time delay circuit is added to the CEZC block, named adjustable delay line (ADL-CEZC). The delayed estimated resonant current is then tied to the optimum delay line block (ODL). The output of the ODL is then capable of prolonging the switching period by changing the on time of the switches (Ton). The output of the ODL is fed into the control block in order to generate the high-side and low-side signals as an input of the gate driver. In addition to the hardware control gates, commands from the FPGA are also have contribution in the control block.

Fig. 9 decomposes the main blocks in the Fig. 8 into sub-blocks also shows a detailed drawing of the main input and output signals inside the block diagram. The voltage $v_F(t)$ is the transformer's primary-side voltage while exhibiting soft switching. $i_{res}(t)$ shows the resonance current of the PT. However, in the PT-based SMPS the resonant current is dependent on the characteristic parameters of the PT and it changes its polarity when either the switches are turned on or their body diodes conduct. Therefore, depending on the operating frequency and temperature of the PT, there is a phase shift between the resonance frequency and the switching voltage, that is defined as ϕ_I in (3), [21]. The signal ZCi_{res} shows the zero crossing resonant current. The CEZC implies a 180° phase shift to the real resonant current. The output of the adjustable delay line (ADL-CEZC) turns on the half-bridge switches. This block is composed of a digitized delay circuit (DDLon) and a FF with 50% square waves in its input and output. The 50% square wave signal fed into to the ODL is delayed by a certain value adjustable with a reference signal. In the end the one-shot pulse signal generated by DDLoff in the output of the ODL turns off the MOSFETs. The high-side and low-side switches are turned on by rising edges of DL-CEZC and $\overline{\text{DL-CEZC}}$ signals, respectively, which are used as clock inputs to the control block FFs. The output of the ODL block is then used to reset the FFs, thereby turning the switches off.

DT is first adjusted for a specific design regarding a certain PT and switching frequency. By adjusting the time-delay for turning the switches off, the frequency of self-oscillation changes. The propagation delay in the control block is assumed negligible in the waveforms shown in Fig. 9.



a: Block digram of self-oscillating loop with optimum phase.



b: Signals with proportional delay for demonstrating the functionality of the optimum phase control method.

Fig. 9: Optimum phase self-oscillating loop and signal waveforms

IV. Results

A prototype has been built and analyzed shown in Fig. 10. Fig. 6 shows designed modular boards for DDL and CEZC blocks. The circuit implemented for CEZC is very similar to one explained in section II-B. Fig. 11 shows signals in the input and output of the DDL module in the setup.

Fig. 12 shows efficiency improvement. The input voltage is 24 V and the load is a 225 Ω resistor in parallel with a 470 μF capacitance. For each specific output voltage the delay has been swept from a minimum value to the maximum value in the range that ZVS is obtained. The starting point for the delay sweep is set to 115.6 kHz in each voltage gain. Therefore, the best phase shift or frequency can be chosen to achieve the maximum possible efficiency as are shown in Fig. 12 with square markers.

Simulation results shown in Fig. 13 for both step-up and step-down converters which shows efficiency improvement by choosing the best phase shift in the loop.

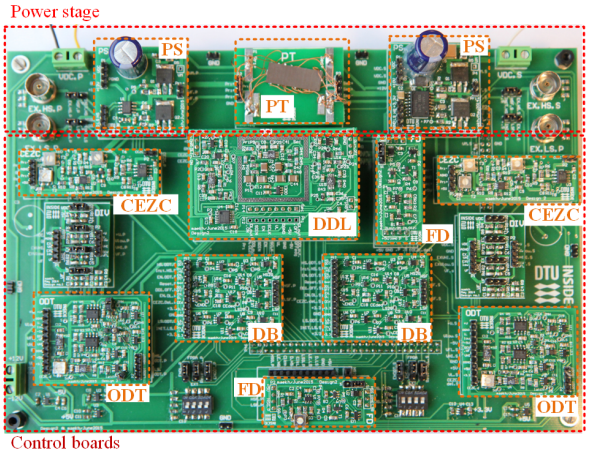


Fig. 10: Prototype buit; bidirectional board.

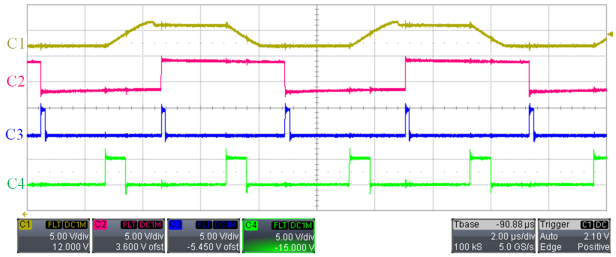


Fig. 11: Signal waveforms where dynamic delay is applied; C1: switching waveform ($v_F(t)$); C2: CEZC as input of DDL block; C3: one-shot pulse as input of DDL block (EDDL$_{in}$); C4: output of DDL (DDL$_{out}$).

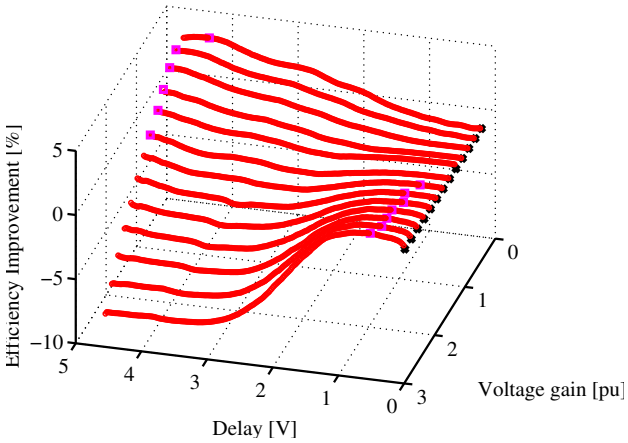


Fig. 12: Experimental results: Efficinecy improvement as a function of voltage gain.

V. Conclusion

General operation of a self-oscillating loop for piezoelectric transformer-based power converters was explained. The designed circuit for operating the transformer together with experimental results were provided. The circuit is based on a

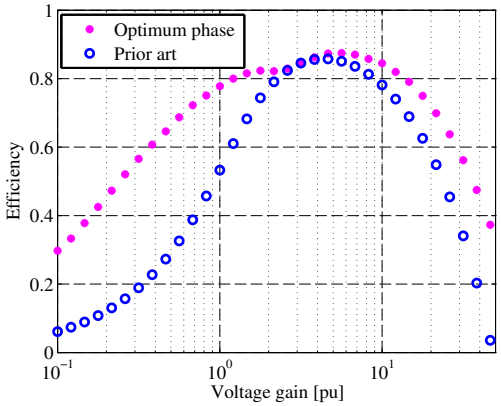


Fig. 13: Simulation results: Efficiency improvement vs. sweep of delay in order to detect the optimum phase (OP) for voltage gains.

new idea for compensating and controlling the total loop phase shift for the self-oscillating PT loop through digital means, in order to achieve and maintain soft switching. This is combined with a resonance current estimation that is able to start and maintain the circuit oscillation. The operation of and cooperation between the analog resonance current estimator and digital phase shift adjustment were presented in detail, together with some insight into the performance of the designed circuit. The concept was proven through the experimental results. 1 ns time step resolution is sufficient for adjusting the phase shift of the loop. The designed circuit is able to follow changes in the resonance frequency of the PT in every cycle. Experimental results showed proof of the concept. Although this method was applied for the PT-based power converters but it has a general application and can also be used for other types of resonant converters. One of the advantages of the presented approach is that the designed hardware can be utilized for different PTs where in previous research; analog self-oscillating loop; the loop should be individually designed for each PT. Another advantage is that implemented method has flexibility for phase shift compensation, but the disadvantage is a complex control method.

ACKNOWLEDGMENT

The authors would like to thank Noliac A/S for supplying the prototype of a piezoelectric transformer as well as "The Danish National Advanced Technology Foundation" for their financial support.

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Appendix J

Resonant power converter with dead-time control of synchronous rectification circuit

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Patent application, DTU-95839/P2086EP00 (January 2016)

Inventors: Marzieh Ekhtiari, Tiberiu-Gabriel Zsurzsan, Michael A. E. Andersen

RESONANT POWER CONVERTER WITH DEAD-TIME CONTROL OF SYNCHRONOUS RECTIFICATION CIRCUIT

The invention relates in a first aspect to a resonant power converter comprising a synchronous rectifier for supplying a DC output voltage. The synchronous rectifier is configured for alternatingly connecting a resonant output voltage to positive and negative DC output nodes via first and second semiconductor switches, respectively, separated by intervening dead-time periods in accordance with first and second rectification control signals. A dead-time controller is coupled to the resonant output voltage or the resonant input voltage and configured for adaptively adjusting lengths of the dead-time periods via the first and second rectification control signals.

BACKGROUND OF THE INVENTION

A sub-group of resonant power converter comprises a piezoelectric transformer as a resonant circuit or resonant tank. Piezoelectric power converters are a viable alternative to traditional magnetics based resonant power converters in numerous voltage or power converting applications such as AC/AC, AC/DC, DC/AC and DC/DC power converter applications. Piezoelectric power converters are capable of providing high isolation voltages and high power conversion efficiencies in a compact package with low EMI radiation. The piezoelectric transformer is normally operated in a narrow frequency band around its fundamental or primary resonance frequency with a matched load coupled to the output of the piezoelectric transformer. The optimum switching frequency or excitation frequency of the piezoelectric power converter shows strong dependence on different parameter such as temperature, load, fixation and age. So-called zero-voltage-switching (ZVS) operation, or soft-switching, of an input driver and/or a synchronous rectification circuit of the piezoelectric power converter is important to avoid prohibitive power losses associated with the respective switching activities of the input driver and/or synchronous rectification circuit. However, synchronous rectification circuits of prior art resonant power converters have utilized a fixed length of the dead-time period, for example tailored to characteristics of a particular piezoelectric transformer at fixed operating conditions. The fixed dead-time period is unable to account for manufacturing tolerances and drift of active and passive electronic components of the resonant power converter, in particular those of a piezoelectric transformer. ´

Hence, the use of fixed dead-time periods leads to increased power consumption of practical resonant power converters where the above-mentioned manufacturing tolerances and drift of active and passive electronic components are inevitable. Hence, it would be advantageous to provide mechanisms for maintaining the desired zero voltage switching (ZVS) properties of the input driver and/or synchronous rectification circuit.

SUMMARY OF THE INVENTION

A first aspect of the invention relates to a resonant power converter comprising:
a first power supply rail for receipt of a positive DC supply voltage and a second power supply rail for receipt of a negative DC supply voltage,
a resonant network comprising an input section for receipt of a resonant input voltage and an output section for supplying a resonant output voltage generated in response to the resonant input voltage,
an input driver configured for supplying the resonant input voltage;
a synchronous rectifier comprising:
a rectifier input coupled to the resonant output voltage,
first and second semiconductor switches controlled by first and second rectification control signals, wherein the synchronous rectifier is configured for alternatingly connecting the resonant output voltage to positive and negative DC output nodes via the first and second semiconductor switches, respectively, separated by intervening dead-time periods in accordance with the first and second rectification control signals;
a first dead-time controller coupled to the resonant output voltage or the resonant input voltage and configured for adaptively adjusting lengths of the dead-time periods via the first and second rectification control signals.

The first dead-time controller is configured to provide adequate length or duration of the dead time periods of the synchronous rectifier to deliver sufficient energy for charging and discharging various capacitances at the output section of the resonant network with the resonant current alternatingly flowing into and out of the resonant network. The capacitances at the output section of the resonant network may com-

prise a capacitance of a secondary section of a piezoelectric transformer and various intrinsic capacitances of the first and second semiconductor switches.

The first dead-time controller is able to maintain zero voltage switching (ZVS) and/or zero current switching (ZCS) of the synchronous rectifier despite temperature drift and variation of component values or parameters of the resonant power converter by adaptively adjusting lengths or durations of the dead-time periods of the synchronous rectifier. Maintaining proper ZVS operation over time minimizes energy consumption involved in the switching activity of the first and second semiconductor switches of the synchronous rectifier. The present inventors have discovered that a dead-time period shorter than required for zero voltage switching causes hard switching of the synchronous rectifier. Likewise, a dead-time period longer than required for zero voltage switching may either cause hard switching of the synchronous rectifier or may cause soft switching of the synchronous rectifier with sub-optimum efficiency. The synchronous rectifier may comprise a half-wave rectifier or a full-wave rectifier.

The resonant power converter may comprise an AC-DC or DC-DC converter topology. The positive and negative DC output nodes of the synchronous rectifier may provide the DC output voltage of the resonant power converter for connecting to a load device, load resistor or load circuit.

The first dead-time controller of the resonant power converter may utilize various features of the resonant output voltage for detecting an optimum length of the dead time period and adaptively adjusting the length of the dead-time period. The dead-time controller may be configured to adjust the length of the dead-time period during every switching cycle of the resonant output voltage based on an instantaneous value thereof. Alternatively, the dead-time controller may be configured to adjust the lengths of dead-time periods during a specific operating condition of the resonant power converter - for example solely during a start-up or initialization phase of the resonant network or solely during steady state operation of the resonant network.

The switching cycle is determined by a selected switching frequency of the resonant power converter. The switching frequency of the resonant power converter may be

set by certain characteristics or tuning of a self-oscillating feedback loop connected around a secondary side circuit of the resonant power converter as discussed in further detail below with reference to the appended drawings.

The synchronous rectifier may comprise a half-bridge or H-bridge driver. The half-bridge driver circuit may comprise a first semiconductor switch and a second semiconductor switch coupled in series between the positive DC supply voltage and the negative DC supply voltage. A midpoint node between the first and second semiconductor switches may be connected to an input of the synchronous rectifier. Hence, according to one embodiment of the resonant power converter, the first semiconductor switch comprises a conducting state connecting the resonant output voltage to the positive DC supply voltage and the second semiconductor switch comprises a conducting state connecting the resonant output voltage to the negative DC supply voltage. In addition, each of the first and the second semiconductor switches resides in a non-conducting or off state during the dead-time periods of the rectification circuit.

According one embodiment of the present resonant power converter, the input driver comprises third and fourth semiconductor switches controlled by first and second driver control signals, respectively. The input driver is configured for alternatingly connecting the resonant input voltage to the positive and negative DC supply voltages through the third and fourth semiconductor switches, respectively, separated by intervening dead-time periods in accordance with the first and second driver control signals. The first driver control signal is configured to switch the third semiconductor switch between a conducting/ON state and a non-conducting/OFF state. The second driver control signal is likewise configured to switch the fourth semiconductor switch between a conducting/ON state and a non-conducting/OFF state. The first and second driver control signals are preferably non-overlapping such that the third semiconductor switch pulls the resonant input voltage towards the positive DC supply voltage via its relatively small on-resistance in the conducting state and the fourth semiconductor switch, subsequent to the intervening dead-time period, pulls the resonant input voltage towards the negative DC supply voltage via its relatively small on-resistance in the conducting state. Hence, during the dead time period of the input driver the resonant input voltage or signal is alternatingly charged and dis-

charged from the positive DC supply voltage to the negative DC supply voltage and vice versa by resonant current flowing through an intrinsic input impedance of the piezoelectric transformer and/or by resonant current flowing through, or out of, a series inductor of the resonant network as discussed in further detail below with reference to the appended drawings. The resonant input signal is effectively clamped to the positive DC supply voltage in a first time period where the third semiconductor switch conducts and the fourth semiconductor switch is non-conducting. Likewise, the resonant input signal is clamped to the negative DC supply voltage in a second time period where the fourth semiconductor switch is conducting and the third semiconductor switch is non-conducting. During the dead-time periods, both the third semiconductor switch and the fourth semiconductor switch are non-conducting. Each of the first, second, third and fourth semiconductor switches may comprise a MOSFET for example a DMOS, PMOS or NMOS device. Each of the first, second, third and fourth semiconductor switches further comprises a control terminal or input such as a gate terminal for receipt of the respective driver control signal or rectification control signal.

As discussed previously, the resonant network may comprise a piezoelectric transformer wherein the input section of the resonant network comprises a primary section of the piezoelectric transformer coupled to the resonant input voltage and the output section of the resonant network comprises a secondary section of the piezoelectric transformer for generating the resonant output voltage.

The switching frequency of the resonant power converter may lie between 75 kHz and 500 kHz such as between 100 kHz and 150 kHz. The resonant power converter may comprise a feedback loop configured to induce self-oscillation around the primary side circuit and/or secondary side circuit of the resonant power converter as discussed in additional detail below. The feedback loop may ensure that a switching frequency of the resonant power converter automatically tracks changing characteristics of the resonant network, e.gl based on a piezoelectric transformer, and electronic circuitry of the primary side or secondary side of the power converter.

According to one embodiment, the dead-time controller utilizes a level or amplitude of the resonant input voltage to detect the respective time instant to switch the first

or the second semiconductor switch to its conducting state. According to another embodiment, the dead-time controller utilizes a waveform shape of the instantaneous resonant input voltage to detect the respective time instants or phases at which to switch the first or second semiconductor to their respective conducting states as discussed in further detail below with reference to the appended drawings.

The dead-time controller may be configured to adjust a phase or timing of the first driver control signal of the first semiconductor switch and a phase or timing of the second driver control signal of the second semiconductor switch to adaptively adjust the duration of the dead-time periods as discussed in further detail below with reference to the appended drawings.

A number of useful embodiments of the present resonant power converter comprise a self-oscillating feedback loop for setting or controlling the switching frequency of the power converter. The self-oscillating feedback loop may be connected around either the primary section or the secondary section of the power converter. The primary side or secondary side self-oscillating feedback loop is efficient in maintain a proper operating point of the resonant power converter despite drift or variation of component values and parameters of the power converter - for example those caused by ageing and temperature variations. The self-oscillating feedback loop may be designed or configured to oscillate at, or proximate to, a fundamental resonance frequency of the resonant network as discussed in further detail below with reference to the appended drawings.

The first dead-time controller may be coupled to the resonant output voltage in one embodiment of the resonant power converter. The resonant power converter further comprises a first self-oscillating feedback loop which comprises a first resonant voltage or current detector coupled to the output section of the resonant circuit and configured to derive a first feedback signal from a resonant voltage or resonant current of the output section. The resonant power converter further comprises a first adjustable delay circuit configured for generating the first and second rectification control signals based on the first feedback signal. The piezoelectric transformer may comprise a separate electrode for supplying the first resonant voltage or current detector with a resonant voltage or current proportional to the resonant output

voltage. Hence, the piezoelectric transformer may comprise:
- a first secondary electrode connected to the secondary section of the piezoelectric transformer for supplying the resonant output voltage; and
- a second secondary electrode embedded in the secondary section for supplying the first feedback signal to the first adjustable delay circuit.

One embodiment of the resonant power converter comprises a first phase shift circuit configured to derive the first and second drive control signals from the first and second rectification control signals by adding respective phase shifts to the first and second rectification control signals. This feature is advantageous in certain applications because the first and second drive control signals are derived/generated in a relatively simple manner from the first and second rectification control signals, respectively, using a small amount of additional components and signal routing as discussed in further detail below with reference to the appended drawings.

In an alternative embodiment, the first dead-time controller is coupled to the resonant input voltage and a self-oscillating feedback loop is connected around the primary section of the power converter. The self-oscillating feedback loop comprises a resonant voltage or current detector coupled to the input section of the resonant circuit and configured to derive a first feedback signal from a resonant voltage or resonant current of the input section; The self-oscillating feedback loop further comprises a first adjustable delay circuit configured for generating the first and second drive control signals based on the first feedback signal. In some of these embodiments, the resonant network comprises a piezoelectric transformer which comprises:
- a first primary electrode connected to the primary section of the piezoelectric transformer for supplying the resonant input voltage; and
- a second primary electrode embedded in the primary section of the piezoelectric transformer for supplying the first feedback signal to the first adjustable delay circuit. One such embodiment comprises a first phase shift circuit configured to derive the first and second drive control signals from the first and second rectification control signals by adding respective phase shifts to the first and second rectification control signals as discussed in further detail below with reference to the appended drawings.

Another alternative embodiment of the resonant power converter comprises two separate and independent self-oscillating feedback loops connected around the primary section or the secondary section, respectively, of the power converter. The presence of such separate self-oscillating feedback loops in the present piezoelectric resonant power converter provides numerous advantages such as an adjustable bi-directional power flow between the DC input voltage and the DC output voltage. The characteristics of this bi-directional power flow can furthermore be very accurately and flexibly controlled by independent digital control or setting of the respective time delays of the first and second adjustable delay circuits as discussed in further detail below with reference to the appended drawings.

One such embodiment of the resonant power converter therefore comprises, in addition to the first self-oscillating feedback loop:

- second self-oscillating feedback loop comprising:

a second resonant voltage or current detector coupled to the input section of the resonant circuit and configured to derive a second feedback signal from a resonant voltage or resonant current of the input section; and a second adjustable delay circuit configured for generating the first and second drive control signals based on the second feedback signal; and

- a second dead-time controller coupled to the resonant input voltage and configured for adaptively adjusting lengths of the dead-time periods of the input driver via the first and second driver control signals. The first adjustable delay circuit may comprise a first digital delay line and a first digital control input for adjusting respective time delays between the first feedback signal and the first and second rectification control signals. The second adjustable time delay circuit may in addition or alternative comprise a second digital delay line and a second digital control input for adjusting respective time delays between the second feedback signal and the first and second driver control signals. Various construction details, programming interfaces etc. of the first and second digital delay lines are discussed in further detail below with reference to the appended drawings.

Each of the first and second adjustable time delay circuits may comprise a digital control input for setting the time delay in the digital domain by a digital processor such as a microprocessor. For this purpose the resonant power converter may

therefore comprise:

a digital processor comprising a first data communication interface connected to at least one of the first and second digital control inputs of the first and second adjustable time delay circuits;

said digital processor being configured to repeatedly compute and apply time delay settings for at least one of:

the first digital delay line for adapting a switching frequency of the first self-oscillating feedback loop to a fundamental resonance frequency of the output section of the resonant circuit; and

the second digital delay line for adapting a switching frequency of the second self-oscillating feedback loop to a fundamental resonance frequency of the input section of the resonant circuit.

The digital processor is configured to:

compute the time delay settings of the first digital delay line to maintain a loop phase shift of substantially 360 degrees, or an integer multiple of 360 degrees, in the first self-oscillating feedback loop; and/or

compute the time delay settings of the second digital delay line to maintain a loop phase shift of substantially 360 degrees, or an integer multiple of 360 degrees, in the second self-oscillating feedback loop.

One embodiment of the first and/or second adjustable time delay circuits has a time step resolution of the first or second digital delay line greater than 10 ns such as greater than 2 ns, or greater than 1 ns, as discussed in further detail below with reference to the appended drawings.

The first dead-time controller may be configured to adjust a phase of the first rectification control signal based on a waveform shape of the resonant output or input voltage and a phase of the second rectification control signal based on the waveform shape of the resonant output or input voltage to adaptively adjust the lengths of the dead-time periods.

A second aspect of the invention relates to a method of adaptively controlling dead-time periods of a synchronous rectifier of a resonant power converter, said method

comprising steps of:

a) generating first and second non-overlapping rectification control signals of the synchronous rectifier in accordance with a resonant output voltage or a resonant input voltage of a resonant network of the resonant power converter, wherein the synchronous rectifier is coupled between positive and negative DC output voltage nodes of the converter,

b) applying the first and second non-overlapping rectification control signals to control inputs of the synchronous rectifier to generate a DC output voltage by alternatingly connecting the resonant output voltage to the positive and negative DC output voltage nodes separated by intervening dead-time periods,

c) monitoring at least one of the resonant output voltage and the resonant input voltage,

d) detecting a feature of a waveform of the resonant output voltage or the resonant input voltage,

f) adjusting lengths of the dead-time periods of the synchronous rectifier based on the detected feature.

According to one embodiment of the present methodology of adaptively controlling dead-time periods, step d) may comprise:

detecting the feature of the waveform in each cycle of the resonant input voltage waveform or detecting the feature of the waveform in each cycle of the resonant output voltage waveform.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described in more detail in connection with the appended drawings, in which:

FIG. 1 shows a simplified schematic circuit diagram of a piezoelectric resonant power converter in accordance with a first embodiment of the invention,

FIG. 2 shows a simplified schematic circuit diagram of an exemplary adjustable delay circuit for application in various embodiments of the present piezoelectric resonant power converters,

FIG. 2A shows a schematic circuit diagram of an exemplary embodiment of the adjustable delay circuit of FIG. 2 based on a digital delay line for application in various embodiments of the present piezoelectric resonant power converters,

FIG. 3 shows a simplified schematic circuit diagram of a piezoelectric resonant power converter in accordance with a second embodiment of the invention,

FIG. 4 shows a schematic block diagram of an exemplary dead-time controller for use in resonant power converters in accordance with various embodiments of the present invention; and

FIG. 5 is a simplified schematic circuit diagram of a piezoelectric resonant power converter in accordance with a third embodiment of the invention,

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following sections various exemplary embodiments of the present resonant power converter are described with reference to the appended drawings. The skilled person will understand that the accompanying drawings are schematic and simplified for clarity and therefore merely show details which are essential to the understanding of the invention, while other details have been left out. Like reference numerals refer to like elements throughout. Like elements will, thus, not necessarily be described in detail with respect to each figure.

FIG. 1 shows a simplified schematic block diagram of a resonant power converter 100 based on a piezoelectric transformer 104 operating as a resonant network of the power converter. The piezoelectric resonant power converter 100 additionally comprises an input driver 103 electrically coupled to an input section or primary section of the piezoelectric transformer 104 for receipt of a resonant input voltage V_{FP}. The resonant input voltage V_{FP} is supplied at an output node or terminal 102 of the input driver 103. Hence, the resonant input voltage V_{FP} is an ac input drive signal at a switching frequency of the power converter. The resonant input voltage V_{FP} may be applied to the input or primary section of the piezoelectric transformer 104 via first and second physical input electrodes of the transformer 104. A driver control circuit 101 is configured to generate appropriately timed gate control signals for the first and second semiconductor switches S_{D1} and S_{D2} of the input driver 103. Each of the first and second semiconductor switches S_{D1} and S_{D2} may comprise a FET for example a NMOS or PMOS transistor. The first and second semiconductor switches S_{D1} and S_{D2} are coupled in cascade such that they jointly form a half-bridge topology of the input driver 103. The second input electrode of the piezoelectric transformer 104 may be connected to a negative DC supply rail of the power converter 100 such

as ground, GND, shared with the input driver 103 as illustrated. The input driver 103 additionally comprises a first power supply rail for receipt of a positive DC supply voltage V_{DD}. Hence, the waveform of the resonant input voltage V_{FP} is determined by a first driver control signal LS_P and a second driver control signal HS_P supplied to the first and second semiconductor switches S_{D1} and S_{D2} through the driver control circuit 101. The first and second input control signals LS_P, HS_P are derived via time delay or phase shift imparted by an optional phase shifter 126 coupled to a first and second rectification control signals LS_S, HS_S of a synchronous rectifier 123 of a secondary side circuit of the resonant power converter as discussed below in further detail. The first and second driver signals LS_P, HS_P are non-overlapping and separated by intervening off periods as discussed below in further detail.

The above-mentioned secondary side circuit of the piezoelectric resonant power converter 100 comprises an output section of the piezoelectric transformer 104, the synchronous rectifier 123, a smoothing capacitor C_L and a converter load R_L connected to a DC output voltage V_{OUT} of the piezoelectric power converter. The output section of the piezoelectric transformer 104 generates the resonant output voltage V_{FS} at an output electrode or electrodes coupled to the secondary section of the piezoelectric transformer 104 in response to the previously discussed application of the resonant input voltage V_{FP} to the primary section of the piezoelectric transformer 104. The resonant output voltage V_{FS} is applied to an input node 122 of the synchronous rectifier 123. The synchronous rectifier 123 comprises first and second semiconductor switches S_{R1} and S_{R2} controlled by the first and second non-overlapping rectification control signals LS_S, HS_S, respectively. The first and second rectification control signals LS_S, HS_S are generated by a self-oscillating feedback loop extending around the secondary circuit of the piezoelectric resonant power converter 100. The non-overlapping property of LS_S, HS_S forces the synchronous rectifier 123 to alternatingly connect the resonant output voltage V_{FS} to the DC output voltage V_{OUT} and ground (GND), serving as the negative DC output voltage in the present embodiment, separated by intervening dead-time periods as controlled by the timings of the first and second rectification control signals LS_S, HS_S. The skilled person will understand that the resonant output voltage V_{FS} is alternatingly connected to the DC output voltage V_{OUT} through a relatively small on-resistance of semiconductor switch S_4 and GND through a relatively small on-resistance of semi-

conductor switch S_{R1}. During the dead-time periods, semiconductor switches S_{R1} and S_{R2} are both placed in non-conducting states or off states to let the resonant output voltage V_{FS} essentially float such that the resonant currents flowing into, or out of, an intrinsic output inductance of the output section of the piezoelectric transformer 104 charges or discharges the input node 122 of the synchronous rectifier 123 either towards V_{OUT} or towards GND. During the dead-time period, the resonant current must charge and discharge output capacitances of the first and second semiconductor switches S_{R1} and S_{R2} and an output capacitance of the secondary section of the piezoelectric transformer 103 as these all are coupled to the input node 122 of the synchronous rectifier 123. The output capacitance associated with the secondary section of the piezoelectric transformer is normally in the range of nF while the output capacitances of typical MOSFETs used as switches S_{R1} and S_{R2} may be around hundreds of pF. Therefore, the dead time period or interval of the synchronous rectifier 123 or the input driver 103 is defined as the time interval of a switching cycle of the resonant input voltage or resonant output voltage where both semiconductor switches, e.g. MOSFETs, are in non-conducting states, i.e. turned off.

The skilled person will understand that the present invention may be applied to magnetics based resonant power converter in a corresponding manner. In such magnetics based resonant power converter, the piezoelectric transformer 104 is replaced by a resonant network typically comprising a number of interconnected capacitors and inductors in accordance with a particular converter topology. The magnetics based resonant power converter may comprise a magnetic transformer galvanically insulating the primary section and the secondary side circuitry of the resonant power converter. The magnetics based resonant power converter may for example comprise a LCC converter topology.

As previously mentioned it is important to have a sufficient duration or length of the intervening dead-time periods between the alternatingly conducting switch states of the first and second semiconductor switches S_{R1} and S_{R2} to provide optimal ZVS operation of the synchronous rectifier 123 for the reasons discussed in significant detail in the applicant's co-pending European patent application No. 15174592.4. In the latter co-pending patent application, optimal ZVS operation is discussed in the context of adjusting the corresponding dead-time periods of the semiconductor

switches of the input driver 103. The ZVS operation eliminates so-called hard switching of the first and and/or second semiconductor switches S_{R1} and S_{R2} of the rectifier which hard switching would lead to a marked increase of the power consumption of the synchronous rectifier 123.

The secondary side circuit of the resonant power converter 100 comprises a dead-time controller comprising an ODT-s block 114 and a cooperating DB-s block 124 which jointly are configured to adaptively adjusting lengths of the dead-time periods of the synchronous rectifier 123 by controlling state switching of the first and second rectifications control signals LS_S, HS_S based on the resonant output voltage $V_{FS.}$ The dead-time controller 114, 124 is capable of adjusting the lengths or durations of the dead-time periods by individually controlling timing or phase of the state transitions of the first and second rectifications control signals LS_S, HS_S applied to the control inputs of the synchronous rectifier 123. The ODT-s block 114 generates a set of control signals to the DB-s block 124 via a signal bus or connection 115. The dead-time controller exploits these control signals to provide adequate length or duration of the dead time periods of the driver circuit to deliver sufficient energy for charging and discharging the output capacitance at the output terminal or node of the output section of the piezoelectric transformer 104. This feature enables zero voltage switching (ZVS) and/or zero current switching (ZCS) of the synchronous rectifier 123 such that energy consumption imparted by the switching activity of the first and second semiconductor switches S_{R1} and S_{R2}.

The dead-time controller 114, 124 may utilize various features of the resonant output voltage V_{FS} for detecting an optimum dead time period of each of the first and second semiconductor switches S_{R1} and S_{R2} and adaptively adjusting the dead-time period. The dead-time controller 114, 124 may in some embodiments be configured to adjust the length of the dead-time period during substantially every switching cycle of the resonant output voltage based on an instantaneous value thereof. This switching cycle is determined by a switching frequency of the resonant power converter. Alternatively, the dead-time controller may be configured to adjust the length of the dead-time period during a specific operating condition of the piezoelectric power converter 100 for example solely during a start-up phase or initialization time of the resonant network or solely during steady state operation of the resonant net-

work as discussed in further detail below with reference to FIG. 4 illustrating an exemplary embodiment of the ODT-s block 114. The adaptive adjustment of the lengths or durations of the dead-time periods reduces energy losses and consequently leads to increased power conversion efficiency of the piezoelectric resonant power converter both during the start-up phase and during steady state operation. The self-oscillating feedback loop of the piezoelectric resonant power converter 100 extends around the secondary side circuit of the power converter. The self-oscillating feedback loop comprises a first resonant voltage or current detector 120 coupled to the output/secondary section of the piezoelectric transformer 104. The first resonant voltage or current detector 120 may be coupled to the piezoelectric transformer 104 via an auxiliary, or second secondary, electrode 121 which provides a resonant voltage or current proportional to the resonant output voltage V_{FS}. The auxiliary, or second secondary, electrode 121 may be embedded in the secondary section of the piezoelectric transformer. The output 119 of the resonant voltage or current detector 120 is digital or binary feedback signal with a frequency corresponding to, or proportional, to the resonant output voltage V_{FS}.

The binary feedback signal is applied to an adjustable delay circuit 125 of the self-oscillating feedback loop. The adjustable delay circuit 125 is configured for deriving the previously discussed first and second rectification control signals LS_S, HS_S of the synchronous rectifier 123 from the first feedback signal. The adjustable delay circuit 125 accomplishes this task by generating a pair of intermediate control signals ODL_{on} and ODL_{off} for the DB-s block 124 as discussed in further detail below with reference to the exemplary embodiment of the adjustable delay circuit 125 and DB-s block 124 depicted on FIGS. 2 and 2A.

The skilled person will understand that the characteristics of the secondary side self-oscillating feedback loop discussed above must satisfy two requirements to produce sustained oscillation in the closed loop. One is that the phase shift through the entire feedback loop should be an integer multiple of 360°; the other requirement is that the loop gain must be greater than unity to start-up oscillation. The former condition is fulfilled by adjusting phase shift through the loop. The latter condition is preferably fulfilled by using a suitable comparator in the resonant voltage or current detector 120. The gain of this comparator can reasonably be considered infinite and therefore its output

voltage, i.e. the first feedback signal, possesses a square wave shape alternatingly saturated to the positive DC supply voltage V_{DD} and the negative DC supply voltage GND.

The first and second drive control signals LS_P, HS_P of the input driver 103 are derived from the first and second rectification control signals LS_S, HS_S via the time delay or phase shift imparted by the phase shifter 126 as previously discussed. In this manner, the first and second drive control signals L_{SP}, H_{SP} may be essentially identical to the first and second rectification control signals, respectively, except for a predetermined phase shift $\Delta\phi$. In this manner, the switching frequency of the resonant input voltage V_{FP} generated by the input driver 103 is forced to, or locked to, the switching frequency of the secondary side self-oscillating feedback loop. The latter feature is advantageous in certain applications because the first and second drive control signals LS_P, HS_P are derived/generated in a relatively simple manner from the first and second rectification control signals, respectively, using a small amount of additional components and signal routing. However, this method of deriving the first and second drive control signals LS_P, HS_P may lead to sub-optimal ZVS properties of the input driver 103 because the timing of the first and second drive control signals LS_P, HS_P is based on the adaptive optimization of the first and second rectification control signals LS_S, HS_S carried out by the dead-time controller 114, 124 and the adjustable delay circuit 125. The optimum timing of the first and second drive control signals LS_P, HS_P may differ from that of the first and second rectification control signals LS_S, HS_S for numerous reasons for example different intrinsic input and output capacitances of the piezoelectric transformer 104, different intrinsic output capacitances between the pair of semiconductor switches S_{D1} and S_{D2} of the input driver and the pair of semiconductor switches S_{R1} and S_{R2} of the synchronous rectifier 123.

The skilled person will appreciate that the dead-time controller 114, 124 is coupled to the resonant output voltage V_{FS} in the present piezoelectric power converter 100 to derive the set of control signals, transmitted via bus 115, to the DB-s block 124 for adjusting the lengths of the dead-time periods of the synchronous rectifier 123. According to the alternative embodiment discussed below with reference to FIG. 3, a corresponding dead-time controller is coupled to the resonant input voltage V_{FP} ra-

ther than the resonant output voltage V_{FS}. In the latter embodiment, the first and second rectification control signals LS_S, HS_S are derived from the first and second drive control signals LS_P, HS_P via an optional phase shifter 326 coupled to the first and second rectification control signals LS_S, HS_S of the input driver. The use of the secondary side self-oscillating feedback loop to control the switching frequency of the present piezoelectric power converter 100 has several advantages. The closed loop control efficiently compensates for the drift or variation of component values and parameters of the power converter for example those caused by ageing and temperature variations. This is achieved because the closed loop control scheme is efficient in keeping the switching frequency of the piezoelectric power converter 100 at a proper operating point of the power converter. This switching frequency typically lies slightly above a fundamental resonant frequency of the piezoelectric transformer 104.

The adjustable delay circuit 125 of the present piezoelectric power converter 100 utilizes a digital delay line to apply a digitized phase shift compensation to the feedback signal to maintain a full feedback loop phase shift of 360° (or a multiple thereof) despite the previously discussed component and parameters variations over time. The time delay imparted by the digital delay line to the binary feedback signal (at the output 119 of the resonant voltage/current detector 120) is digitally controllable via a digital control input of the adjustable delay circuit 125 through a data communication interface 135. The data communication interface 135 is connected to a digital controller 130 that is configured to program or write a desired time delay to the adjustable delay circuit as discussed in further detail below with reference to FIG. 2A. The digital controller 130 may comprise a software programmable device such as a microprocessor or hard-wired digital logic circuitry for example comprising a digital sequential and combinational logic. The digital controller 130 may be programmed or implemented by a FPGA device or fabricated as an ASIC - for example using sub-micron CMOS technology.

FIG. 2 shows a simplified schematic circuit diagram of an exemplary embodiment of the adjustable delay circuit 125 and the DB-s block 124 which also forms part of the dead-time controller 124 as discussed above. The skilled person will appreciate that the adjustable delay circuits of the other embodiments of the present resonant power converters 300, 500 as discussed below in connection with FIG. 3 and FIG. 5 may be sub-

stantially identical to the adjustable delay circuit 125. The ODL block 125 is composed of two sub-blocks 201, 203 designated ODL_{on} and ODL_{off}, respectively. The previously discussed binary feedback signal is applied to the input of the adjustable delay circuit 125 and gets delayed by ODL_{on} to turn on, i.e. switching to the conducting state, each of the first and second semiconductor switches S_{R1} and S_{R2} at its rising edge. The output of the ODL_{on} sub-block 201 is tied to the ODL_{off} and imposes additional time delays to the binary feedback signal to turn off, i.e. switching to a non-conducting state, each of the first and second semiconductor switches S_{R1} and S_{R2} at each rising edge of its output pulses. The time delay applied by the ODL_{off} sub-block 203 defines the on-time or conducting time period of the first and second semiconductor switches S_{R1} and S_{R2}. The DB-s block 124 is controlling the final waveforms of the first and second rectification control signals LS_S, HS_S. The time delay span of the adjustable delay circuit 125 may correspond to at least one half–cycle of the either the resonant input voltage or the resonant output voltage. In the present embodiment, signal Ref applied to the input of an optional fixed time delay (FTD) circuit increases the time delay of the adjustable delay circuit 125 in certain predetermined steps to ensure that the time delay span of the circuit 125 covers at least the one half–cycle of the either the resonant input voltage or the resonant output voltage.

The configuration or topology of the adjustable delay circuit 125 provides a digitally programmable or settable time delay of the dead-time periods with very high resolution as explained in further detail below with reference to the detailed schematic of FIG. 2A. The inventors have achieved a time resolution down to 1 ns in an experimental prototype of the present piezoelectric power converter 100. The high time resolution makes it possible to accurately control the time delay added to the secondary side self-oscillating feedback loop and/or to the primary side self-oscillating feedback loop as discussed below. In return, this feature allows the digital controller 130 to very accurately adapt or adjust the switching frequency of the self-oscillating loop to changes of the operating point, e.g. the fundamental resonance frequency, of the piezoelectric transformer 104.

FIG. 2A shows a schematic circuit diagram 205 of an exemplary embodiment of the adjustable delay circuit blocks DDL-ON 205a and DDL-OFF 205b of FIG. 2 based on the digital delay line. The adjustable delay circuit block 205 comprises a resetta-

ble integrator build around operational amplifier 211 generating a saw tooth waveform to the inverting input of a comparator 213. The resettable integrator uses capacitor C_F as integration element and is reset by switch D1 via a control network steered by an inverting output. The non-inverting input of the comparator 213 is supplied with an adjustable reference voltage V_{Ref} generated by a programmable D/A converter 207. The programmable D/A converter 207 may have a resolution between 12 and 18 bits for example 16 bits as illustrated. The level of the reference voltage V_{Ref} is set by a digital control input 215 of the programmable D/A converter 207. This digital control input 215 is connected to the previously discussed digital controller 130 via the data communication/programming interface or bus 135. The data communication bus 135 may comprise a SPI compatible data bus or any other suitable data bus. The high resolution of the programmable D/A converter 207 enables a very small step size of the level of the reference voltage V_{Ref} such that the latter can be very accurately set to a desired voltage. The small step size of the level of the reference voltage V_{Ref} allows the delay time of the output signal DDL_{out} to in response be adjusted in very small time steps such as time steps of 10 ns or smaller or 1 ns or smaller depending *inter alia* on the selected resolution of the programmable D/A converter 207.

Waveform graph 250 shows respective exemplary waveforms of the input signal DDL_{in} and output signal DDL_{out} of the adjustable delay circuit block DDL-ON 205. The graph 250 finally shows a corresponding waveform of the internal control signal $EDDL_{in}$.

FIG. 3 shows a simplified schematic block diagram of a piezoelectric resonant power converter 300 in accordance with a second embodiment of the invention. The piezoelectric resonant power converter 300 largely comprises corresponding circuit blocks and features to those of the first embodiment of the piezoelectric resonant power converter 100 discussed above. However, the piezoelectric resonant power converter 300 comprises a self-oscillating feedback loop connected around a primary side circuit of the power converter 100 in contrast to the self-oscillating feedback loop of the previous piezoelectric resonant power converter 100 which was connected around the secondary circuit of the converter.

The primary side circuit of the resonant power converter 300 comprises a dead-time controller comprising an ODT-p block 314 and a cooperating DB-p block 324 which jointly are configured to adaptively adjusting lengths of the dead-time periods of the input driver 303 by controlling state switching of first and second driver control signals LS_P, HS_P based on the resonant output voltage $V_{FS.}$ The dead-time controller 314, 324 is thereby capable of adjusting the lengths or durations of the dead-time periods of input driver 303 by individually controlling timing or phase of the state transitions of the first and second driver control signals LS_P, HS_P applied to the control inputs of the input driver. The input driver 303 comprises semiconductor switches S_{D1} and S_{D2} which are both placed in non-conducting states, or off states, during each dead-time period to let the resonant input voltage V_{FP} essentially float such that resonant currents flowing into, or out of, an intrinsic input inductance of the primary section of the piezoelectric transformer 304 charges or discharges the resonant input voltage V_{FP} either towards V_{DC} or towards GND. During each the dead-time period, the resonant current must either charge or discharge the output capacitances of the first and second semiconductor switches S_{D1} and S_{D2} and an input capacitance of the primary section of the piezoelectric transformer 303 as these all are coupled to the deriver output node 102. The role of the ODT-p block 314 and cooperating DB-p block 324 is provide an adaptable and optimum length of the dead-time periods of the input driver 303 in a manner largely similar to the adaptable and optimum dead-time period of the synchronous rectifier 123 of the previous embodiment of the resonant power converter 100. As mentioned previously, the operation theory and principles of the dead-time controllers are discussed in significant detail in the applicant's co-pending European patent application No. 15174592.4. FIG. 4 is illustrating an exemplary embodiment of the ODT-p block 314.

The primary side self-oscillating feedback loop comprises a resonant voltage or current detector 320 coupled to the input /primary section of the piezoelectric transformer 304. The first resonant voltage or current detector 320 may be coupled to the piezoelectric transformer 304 via an auxiliary, or second primary, electrode 321 which provides a resonant voltage or current proportional to the resonant input voltage V_{FP}. The output 319 of the resonant voltage or current detector 320 is digital or binary feedback signal with a frequency corresponding to, or proportional, to the resonant output voltage V_{FP}. The binary feedback signal is applied to an adjustable

delay circuit 325 of the primary side self-oscillating feedback loop. The adjustable delay circuit 125 derives the previously discussed first and second drive control signals LS_P, HS_P from the binary feedback signal in a similar manner to the operation of the previously discussed adjustable delay circuit 125 of the first embodiment of the power converter 100. The skilled person will understand that the characteristics of the primary side self-oscillating feedback loop must satisfy same two requirements as those discussed above in respect of the secondary side self-oscillating feedback loop discussed above to produce and maintain sustained oscillation in the closed loop. The resonant power converter 300 furthermore comprises a digital controller 330 that is configured to program or write a desired time delay to the adjustable delay circuit 325 via a data bus or interface 335 in a similar manner to the one discussed above in connection with the previous embodiment of the invention.

The first and second rectification control signals LS_S, HS_S of the synchronous rectifier 323 are derived from the first and second drive control signals LS_P, HS_P of the input driver 303 via a time delay or phase shift imparted by a phase shifter 326. In this manner, the first and second rectification control signals LS_S, HS_S are derived by the primary side connected dead-time controller 325 which is coupled to the resonant input voltage V_{FP} rather than the resonant output voltage V_{FS}. The first and second rectification control signals may be essentially identical to the first and second drive control signals, respectively, except for a predetermined phase shift $\Delta\phi$ generated by the phase shifter 326. Thereby, the switching frequency of the resonant output voltage V_{FS} applied to the input of the synchronous rectifier 323 is forced to, or locked to, the switching frequency of the primary side self-oscillating feedback loop. The latter feature is advantageous in certain applications because the first and second rectification control signals LS_S, HS_S are derived/generated in a relatively simple manner from the first and second drive control signals, respectively, using a small amount of additional components and signal routing. The role of the primary side self-oscillating feedback loop of the present converter 300 is to control the switching frequency of the piezoelectric power converter 300 and preferably maintain the switching frequency of the converter at a substantially optimal frequency of the piezoelectric transformer 304 despite drift and variation of component values and parameters of the power converter 300 - for example caused by ageing and/or temperature variations.

FIG. 4 shows a schematic block diagram of an exemplary embodiment of the dead-time controllers 114, 314, 514 of the piezoelectric power converters 100, 300, 500. The dead-time controller 414 comprises *inter alia* a steady-state controller 624 and a start-up controller 634 and a control circuit 644 (OTD C). The steady-state controller 624 is adapted to generate appropriately timed first and second driver control signals HS_G, LS_G for the either the input driver 103 or the synchronous rectifier 323 of the piezoelectric power converters 100, 300. The start-up controller 634 is adapted to generate appropriately timed first and second driver control signals HS_G, LS_G or first and second rectification control signals LS_S, HS_S during the initialization time or start-up time of the piezoelectric power converters 100, 300. The operation theory and operation principles of the dead-time controller 514 are discussed in significant detail in the applicant's co-pending European patent application No. 15174592.4 and will not be repeated here.

FIG. 5 is a simplified schematic circuit diagram of a piezoelectric resonant power converter 500 in accordance with a third embodiment of the invention. The piezoelectric resonant power converter 500 comprises two separate self-oscillating feedback loops connected around the primary section of the converter and the secondary section of the converter, respectively. The piezoelectric resonant power converter 500 furthermore comprises two separate dead-time controllers. A first dead-time controller is connected to the resonant output voltage and comprises an ODT-s block 514 and a cooperating DB-s block 524 which jointly are configured to adaptively adjusting lengths of the dead-time periods of the synchronous rectifier 523 by controlling state switching of first and second driver control signals LS_P, HS_P based on the resonant output voltage $V_{FS.}$ The primary side circuit of the resonant power converter 500 comprises a second dead-time controller comprising an ODT-p block 514 and a cooperating DB-p block 524p which jointly are configured to adaptively adjusting lengths of the dead-time periods of the input driver 503 by controlling state switching of first and second driver control signals LS_P, HS_P based on the resonant input voltage $V_{FP.}$ The skilled person will understand that the first dead-time controller may be substantially identical to the dead-time controller discussed above in connection with the first embodiment of the piezoelectric power converter 100 and

that the second dead-time controller may be substantially identical to the dead-time controller discussed above in connection with the second embodiment of the piezoelectric power converter 300. The use of two separate dead-time controllers in the present piezoelectric resonant power converter 500 provides separate optimization of the lengths of the dead-time periods of synchronous rectifier 523 and the lengths of the dead-time periods of the input driver 503. This may be a significant advantage for numerous types of resonant power converters because the optimum lengths of these different dead-time periods typically differ for example due to different intrinsic input and output capacitances of the piezoelectric transformer 504 etc. as briefly discussed above.

The first self-oscillating feedback loop of the piezoelectric resonant power converter 500 comprises a first resonant voltage or current detector 520s coupled to an output/secondary section of the piezoelectric transformer 504. The first resonant voltage or current detector 520s may be coupled to the piezoelectric transformer 504 via an auxiliary, or second secondary, electrode as discussed above in connection with FIG. 1. The output of the resonant voltage or current detector 520s is a digital or binary feedback signal with a frequency corresponding to, or proportional, to the resonant output voltage V_{FS}. The binary feedback signal is applied to a first adjustable delay circuit 525s of the self-oscillating feedback loop which may be identical to the previously discussed adjustable delay circuit 125 of the first power converter embodiment 100. The second, or primary side, self-oscillating feedback loop comprises a second resonant voltage or current detector 520p coupled to the input/primary section of the piezoelectric transformer 504. The second resonant voltage or current detector 520p may be coupled to the piezoelectric transformer 504 via an auxiliary, or second primary, electrode as discussed above in connection with FIG. 3. The output of the resonant voltage or current detector 520p is a digital or binary feedback signal with a frequency corresponding to, or proportional, to the resonant input voltage V_{FP}. The binary feedback signal is applied to a second adjustable delay circuit 525p of the primary side self-oscillating feedback loop. The second adjustable delay circuit 525p derives the previously discussed first and second drive control signals LS_P, HS_P from the binary feedback signal in a similar manner to the operation of the previously discussed adjustable delay circuit 325 of the second embodiment of the power converter 300. The skilled person will understand operational

characteristics and features of the first self-oscillating feedback loop may be substantially identical to those of the self-oscillating feedback loop discussed above in connection with the first embodiment of the piezoelectric power converter 100 and that the operational characteristics and features of the second self-oscillating feedback loop may be substantially identical to those of the self-oscillating feedback loop discussed above in connection with the second embodiment of the piezoelectric power converter 300.

The presence of two separate self-oscillating feedback loops within the present piezoelectric resonant power converter 500 provides numerous advantages such as an adjustable bi-directional power flow between the DC input voltage and the DC output voltage. This bi-directional power flow can furthermore be very accurately and flexibly controlled by the digital control, via the digital controller 530s, of the time delay through programming of the first adjustable delay circuit 525s, e.g. with 10 ns or better resolution such as better than 1 ns. The control of the bi-directional power flow is a significant advantage because this feature allows efficient driving of inductive loads and seamless integration in numerous smart-grid applications and networks. The piezoelectric resonant power converter 500 furthermore comprises first and second digital controllers 530s, 530p. The first digital controller 530s is configured to program or write a desired time delay to the first adjustable delay circuit 525s via a first data bus or interface 535s in a similar manner to the one discussed above in connection with FIG. 1. The second digital controller 530p is configured to program or write a desired time delay to the first adjustable delay circuit 525s via a second data bus or interface 535p in a similar manner to the one discussed above in connection with FIG. 3. The first and second digital controllers 530p, 530s may be physically separate circuits or devices which has the advantage of enabling galvanic isolation between the primary side and secondary side circuits of the piezoelectric resonant power converter 500. However, in alternative embodiments of power converter 500, the first and second digital controller 530p, 530s may be integrated or fused to form a single physical circuit or device connected to both of the first and second data busses or interfaces 535s, 535p. This embodiment of the power converter 500 may lower component costs and space requirements of the power converter.

CLAIMS

1. A resonant power converter comprising:
a first power supply rail for receipt of a positive DC supply voltage and a second power supply rail for receipt of a negative DC supply voltage,
a resonant network comprising an input section for receipt of a resonant input voltage and an output section for supplying a resonant output voltage generated in response to the resonant input voltage,
an input driver configured for supplying the resonant input voltage;
a synchronous rectifier comprising:
a rectifier input coupled to the resonant output voltage,
first and second semiconductor switches controlled by first and second rectification control signals, wherein the synchronous rectifier is configured for alternatingly connecting the resonant output voltage to positive and negative DC output nodes via the first and second semiconductor switches, respectively, separated by intervening dead-time periods in accordance with the first and second rectification control signals;
a first dead-time controller coupled to the resonant output voltage or the resonant input voltage and configured for adaptively adjusting lengths of the dead-time periods via the first and second rectification control signals.

2. A resonant power converter according to claim 1, wherein the input driver comprises third and fourth semiconductor switches controlled by first and second driver control signals; wherein the input driver is configured for alternatingly connecting the resonant input voltage to the positive and negative DC supply voltages through the third and fourth semiconductor switches, respectively, separated by intervening dead-time periods in accordance with the first and second driver control signals.

3. A resonant power converter according to any of the preceding claims, wherein the resonant network comprises a piezoelectric transformer;
wherein the input section of the resonant network comprises a primary section of the piezoelectric transformer coupled to the resonant input voltage and the output section of the resonant network comprises a secondary section of the piezoelectric

transformer for generating the resonant output voltage.

4. A resonant power converter according to any of the preceding claims, wherein the first dead-time controller is coupled to the resonant output voltage; said resonant power converter further comprising:
a first self-oscillating feedback loop comprising:
a first resonant voltage or current detector coupled to the output section of the resonant circuit and configured to derive a first feedback signal from a resonant voltage or resonant current of the output section; and
- a first adjustable delay circuit configured for generating the first and second rectification control signals based on the first feedback signal.

5. A resonant power converter according to claims 3 and 4, wherein the piezoelectric transformer comprises:
- a first secondary electrode connected to the secondary section of the piezoelectric transformer for supplying the resonant output voltage; and
- a second secondary electrode embedded in the secondary section for supplying the first feedback signal to the first adjustable delay circuit.

6. A resonant power converter according to claim 5, further comprising:
a first phase shift circuit configured to derive the first and second drive control signals from the first and second rectification control signals by adding respective phase shifts to the first and second rectification control signals.

7. A resonant power converter according to any of claims 1-3, wherein the first dead-time controller is coupled to the resonant input voltage; said resonant power converter further comprising:
a self-oscillating feedback loop comprising:
a resonant voltage or current detector coupled to the input section of the resonant circuit and configured to derive a first feedback signal from a resonant voltage or resonant current of the input section; and
- a first adjustable delay circuit configured for generating the first and second drive control signals based on the first feedback signal.

8. A resonant power converter according to claims 3 and 7, wherein the piezoelectric transformer comprises:
- a first primary electrode connected to the primary section of the piezoelectric transformer for supplying the resonant input voltage; and
- a second primary electrode embedded in the primary section of the piezoelectric transformer for supplying the first feedback signal to the first adjustable delay circuit.

9. A resonant power converter according to claim 8, further comprising:
a first phase shift circuit configured to derive the first and second drive control signals from the first and second rectification control signals by adding respective phase shifts to the first and second rectification control signals.

10. A resonant power converter according to any of claims 4-6, further comprising:
- second self-oscillating feedback loop comprising:
a second resonant voltage or current detector coupled to the input section of the resonant circuit and configured to derive a second feedback signal from a resonant voltage or resonant current of the input section; and
- a second adjustable delay circuit configured for generating the first and second drive control signals based on the second feedback signal; and
- a second dead-time controller coupled to the resonant input voltage and configured for adaptively adjusting lengths of the dead-time periods of the input driver via the first and second driver control signals.

11. A resonant power converter according to any of claims 4-10, wherein the first adjustable delay circuit comprises a first digital delay line and a first digital control input for adjusting respective time delays between the first feedback signal and the first and second rectification control signals; and/or
the second adjustable time delay circuit comprises a second digital delay line and a second digital control input for adjusting respective time delays between the second feedback signal and the first and second driver control signals.

12. A resonant power converter according to claim 11, further comprising:
- a digital processor comprising a first data communication interface connected to at

least one of the first and second digital control inputs of the first and second adjustable time delay circuits;

said digital processor being configured to repeatedly compute and apply time delay settings for at least one of:

the first digital delay line for adapting a switching frequency of the first self-oscillating feedback loop to a fundamental resonance frequency of the output section of the resonant circuit; and

the second digital delay line for adapting a switching frequency of the second self-oscillating feedback loop to a fundamental resonance frequency of the input section of the resonant circuit.

13. A resonant power converter according to claim 12, wherein the digital processor is configured to:

compute the time delay settings of the first digital delay line to maintain a loop phase shift of substantially 360 degrees, or an integer multiple of 360 degrees, in the first self-oscillating feedback loop; and/or

compute the time delay settings of the second digital delay line to maintain a loop phase shift of substantially 360 degrees, or an integer multiple of 360 degrees, in the second self-oscillating feedback loop.

14. A method of adaptively controlling dead-time periods of a synchronous rectifier of a resonant power converter, said method comprising steps of:

a) generating first and second non-overlapping rectification control signals of the synchronous rectifier in accordance with a resonant output voltage or a resonant input voltage of a resonant network of the resonant power converter, wherein the synchronous rectifier is coupled between positive and negative DC output voltage nodes of the converter,

b) applying the first and second non-overlapping rectification control signals to control inputs of the synchronous rectifier to generate a DC output voltage by alternatingly connecting the resonant output voltage to the positive and negative DC output voltage nodes separated by intervening dead-time periods,

c) monitoring at least one of the resonant output voltage and the resonant input voltage,

d) detecting a feature of a waveform of the resonant output voltage or the resonant

input voltage,

f) adjusting lengths of the dead-time periods of the synchronous rectifier based on the detected feature.

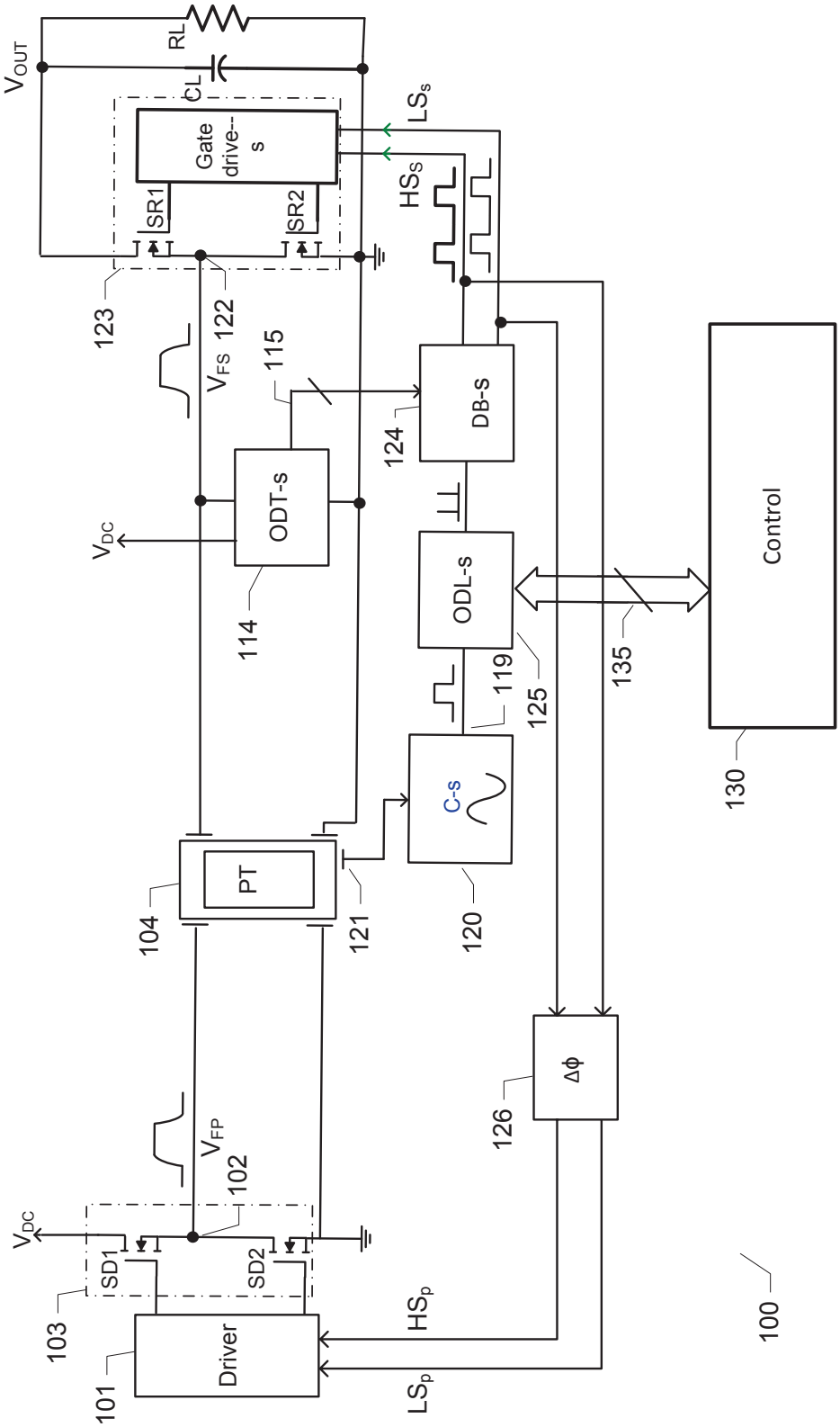
15. A method of adaptively controlling dead-time periods of a synchronous rectifier according to claim 15, wherein step d) comprises:

detecting the feature of the waveform in each cycle of the resonant input voltage waveform or detecting the feature of the waveform in each cycle of the resonant output voltage waveform.

ABSTRACT

The invention relates in a first aspect to a resonant power converter comprising a synchronous rectifier for supplying a DC output voltage. The synchronous rectifier is configured for alternatingly connecting a resonant output voltage to positive and negative DC output nodes via first and second semiconductor switches, respectively, separated by intervening dead-time periods in accordance with first and second rectification control signals. A dead-time controller is coupled to the resonant output voltage or the resonant input voltage and configured for adaptively adjusting lengths of the dead-time periods via the first and second rectification control signals.

(FIG. 1 for publication)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CL
Gate drive--s
SR1
SR2
LS_s
HS_S
123
122
V_{FS}
115
DB-s
124
ODT-s
V_{DC}
114
ODL-s
119
125
135
Control
130
C-s
120
PT
104
121
126
Δφ
V_{FP}
102
V_{DC}
SD1
SD2
103
Driver
101
HS_p
LS_p
100

FIG. 1

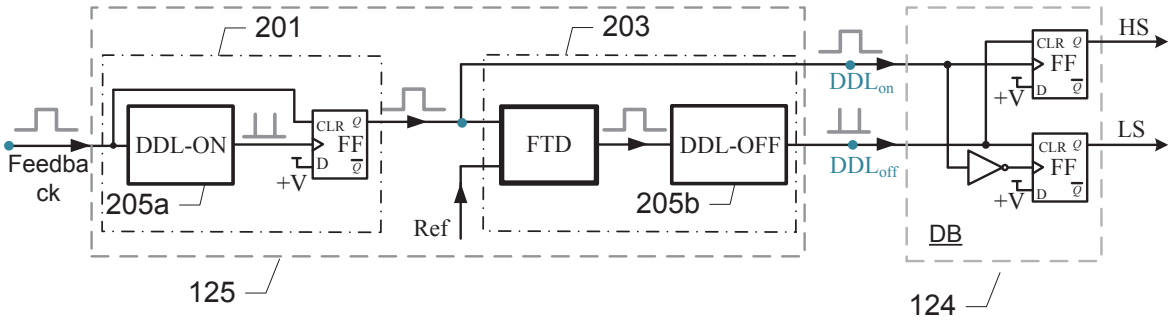
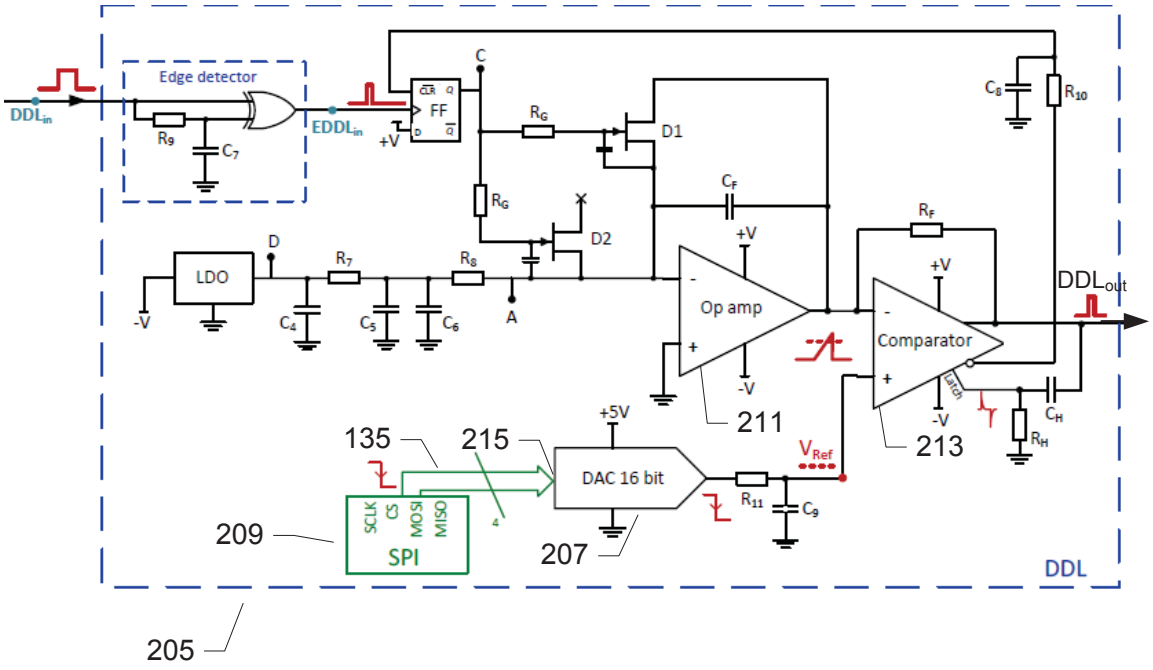

201
203
Feedba
ck
DDL-ON
CLR
FF
D
+V
205a
FTD
DDL-OFF
205b
Ref
DDL$_{on}$
DDL$_{off}$
HS
LS
DB
125
124

FIG. 2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Edge detector
R9
C7
EDDL_in
+V
C
FF
RG
D1
CF
C8
R10
RG
D2
RF
D
LDO
-V
R7
R8
C4
C5
C6
A
+V
Op amp
-V
211
Comparator
213
DDL_out
+5V
135
215
DAC 16 bit
VRef
R11
C9
CH
RH
209
SCLK
CS
MOSI
MISO
SPI
207
DDL
205

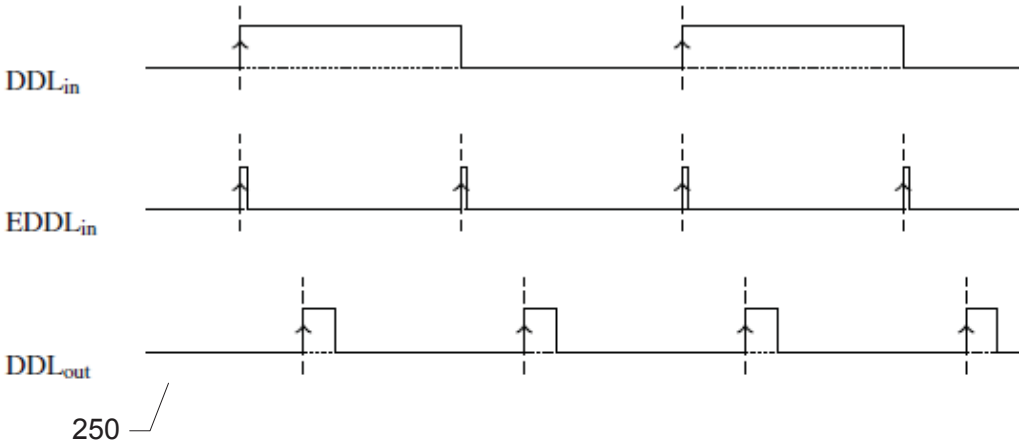
DDL_in
EDDL_in
DDL_out
250

FIG. 2A

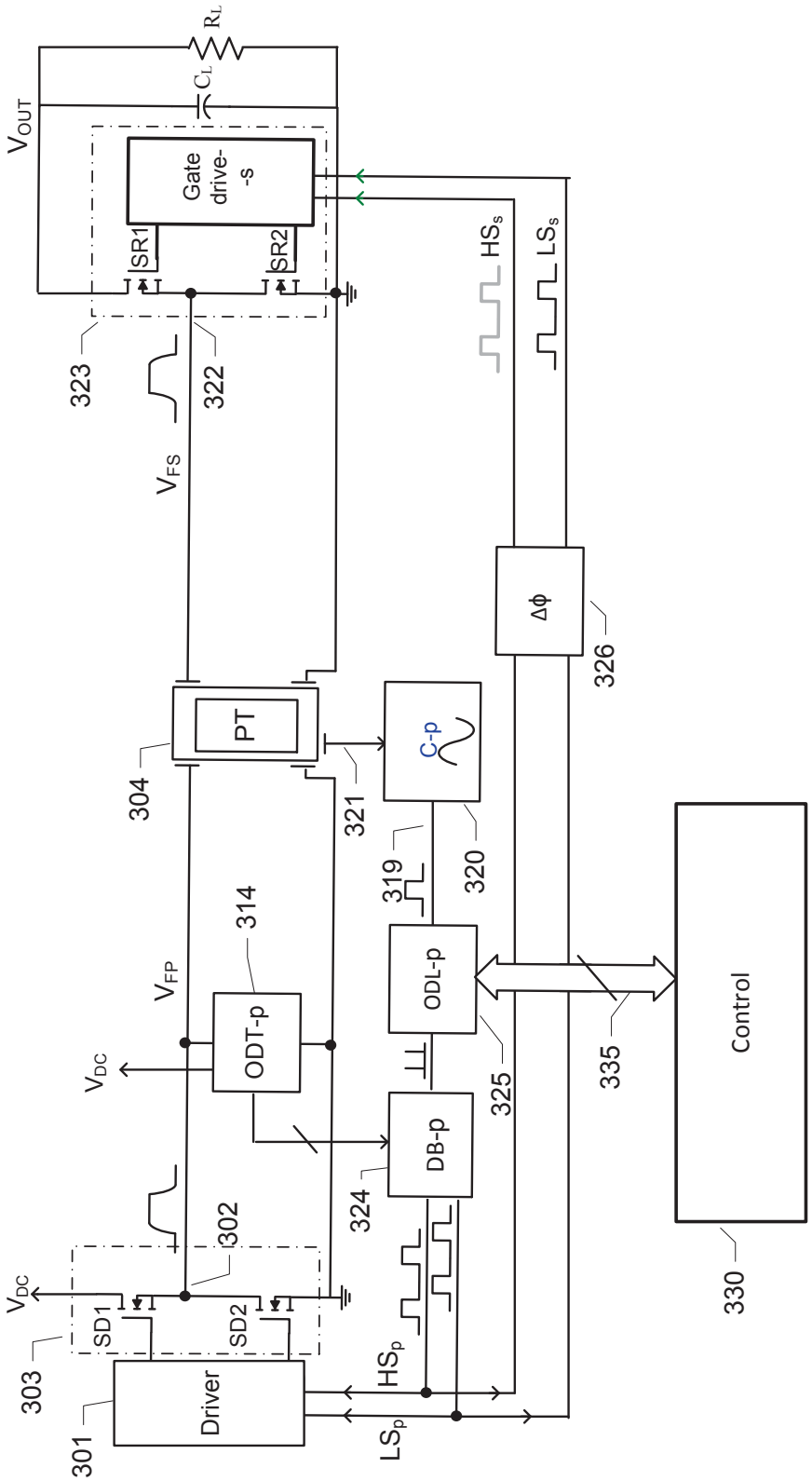
V_{OUT}
C_L
R_L
Gate drive-s
SR1
SR2
323
322
V_{FS}
HS_s
LS_s
PT
304
321
C-p
319
320
$\Delta\phi$
326
314
V_{FP}
ODT-p
ODL-p
V_{DC}
325
335
Control
DB-p
324
302
V_{DC}
SD1
SD2
303
Driver
301
HS_p
LS_p
330
300

FIG. 3

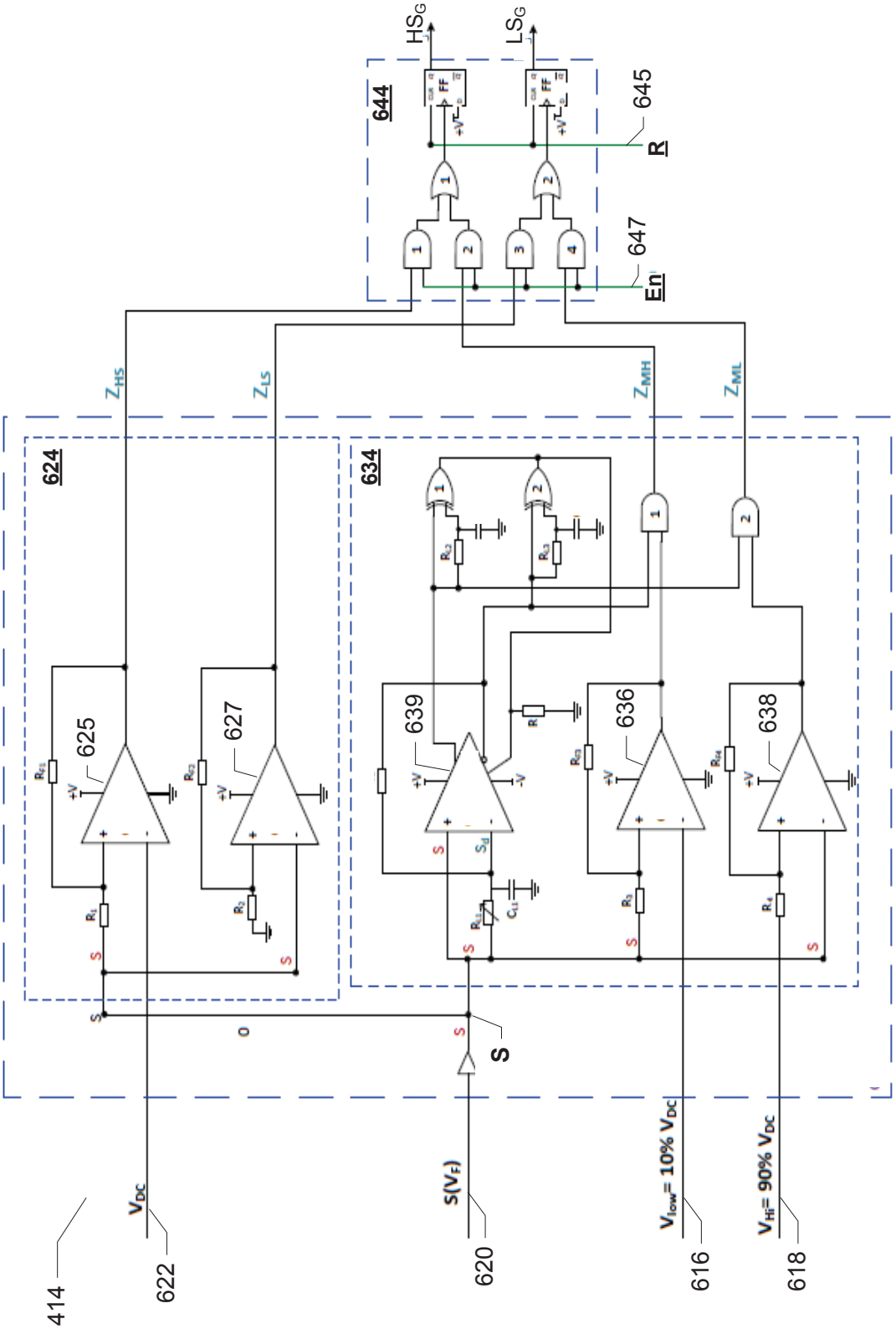
HSG
LSG
644
645
R
647
En
ZHS
ZLS
ZMH
ZML
624
634
625
627
639
636
638
S
0
S
S(VF)
VDC
Vlow= 10% VDC
VHi= 90% VDC
414
622
620
616
618

FIG. 4

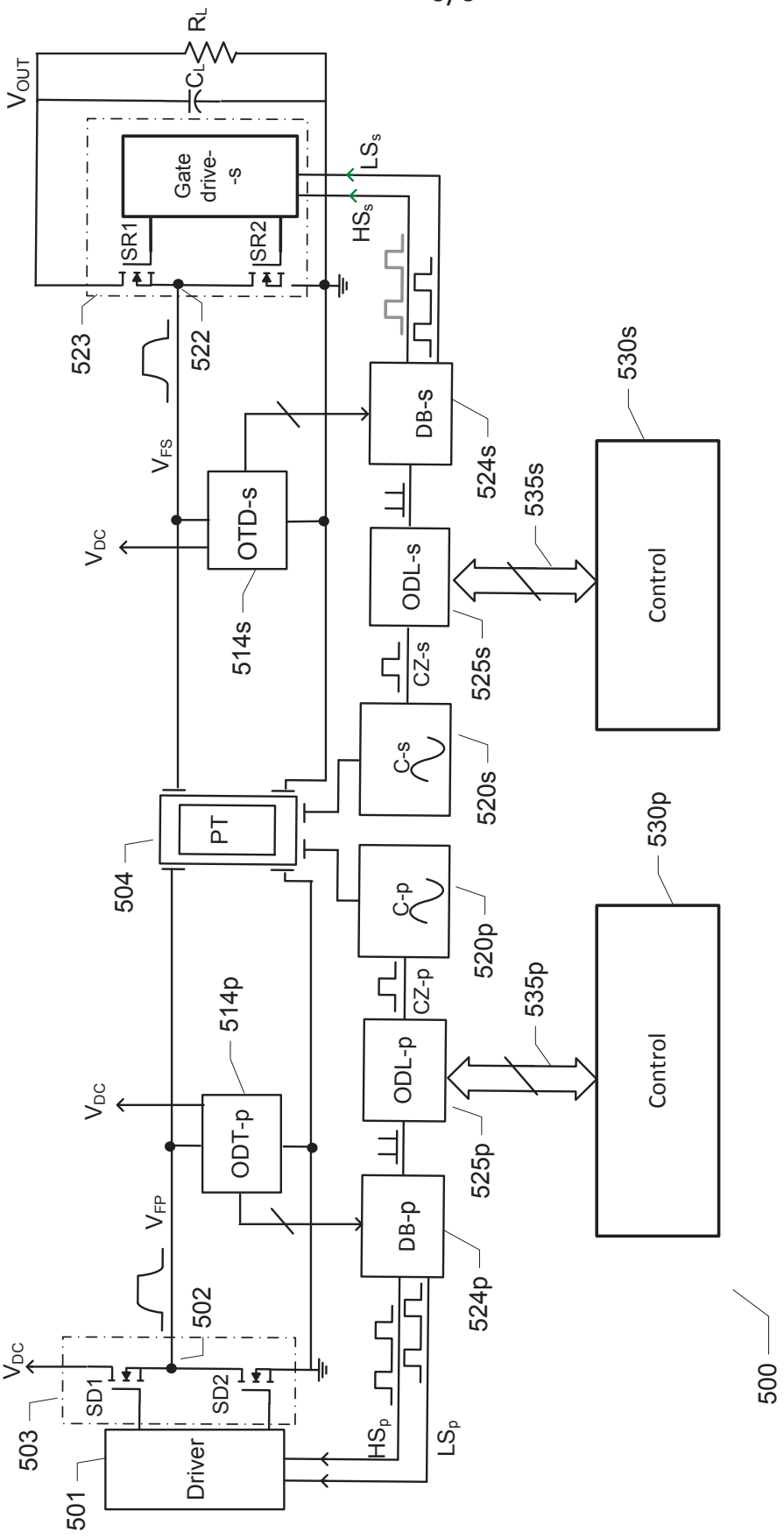
V_{OUT}
R_L
C_L
Gate drive-s
SR1
SR2
LS_s
HS_s
523
522
V_{FS}
V_{DC}
OTD-s
514s
DB-s
524s
530s
535s
ODL-s
525s
CZ-s
Control
C-s
520s
PT
504
C-p
520p
530p
514p
ODT-p
V_{FP}
ODL-p
535p
525p
DB-p
524p
502
503
SD1
SD2
Driver
501
HS_p
LS_p
500

FIG. 5

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